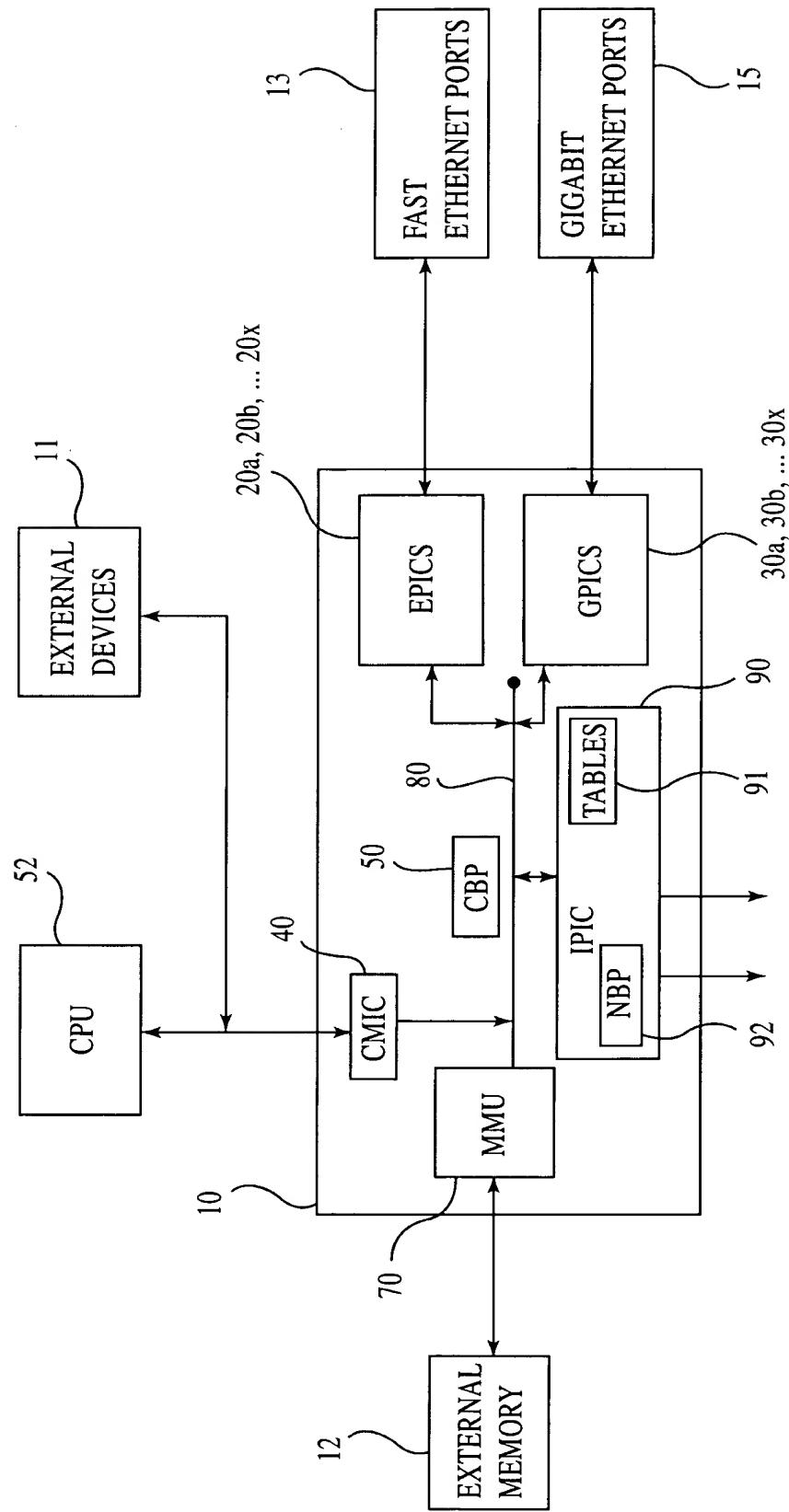




Fig.1



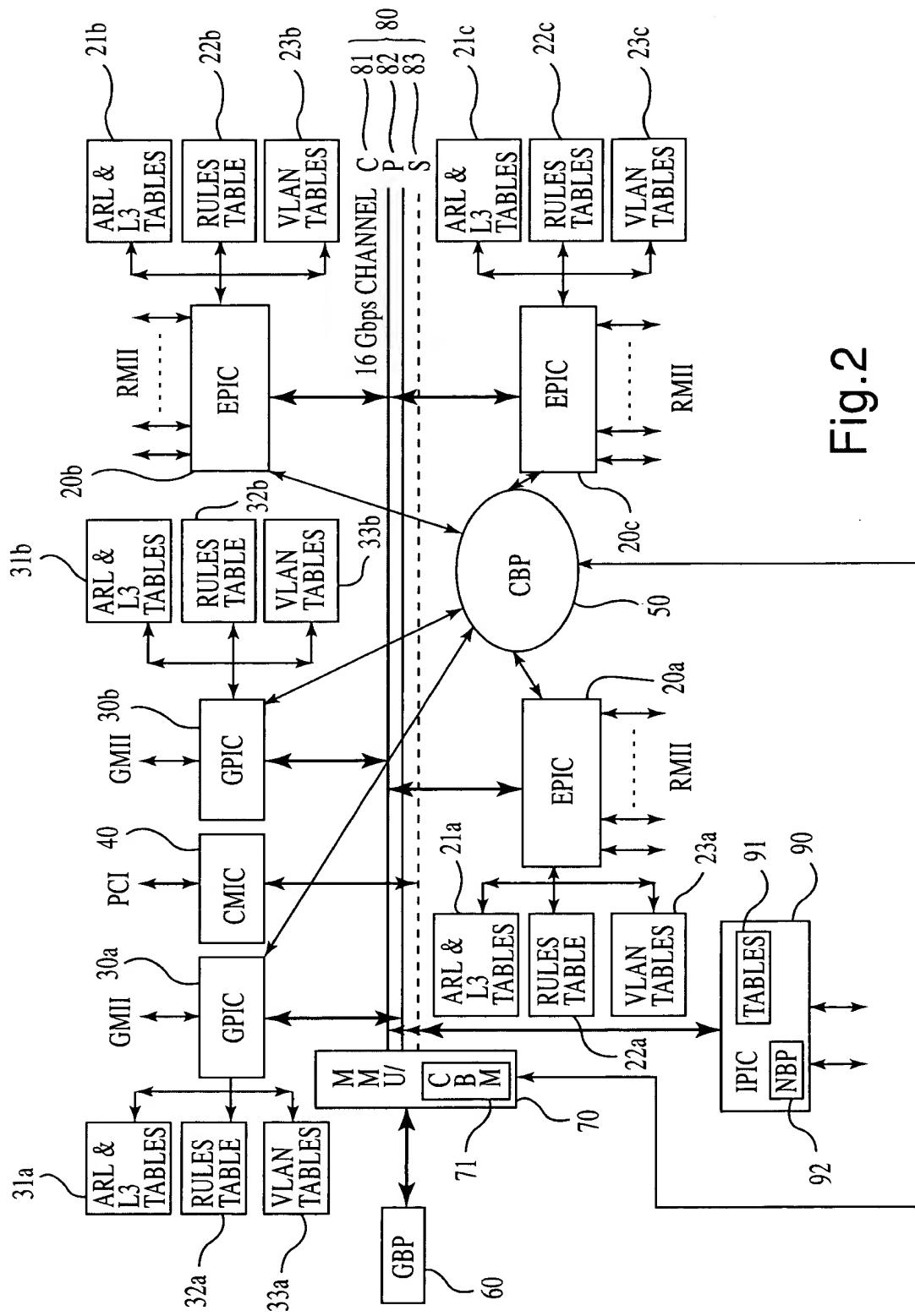
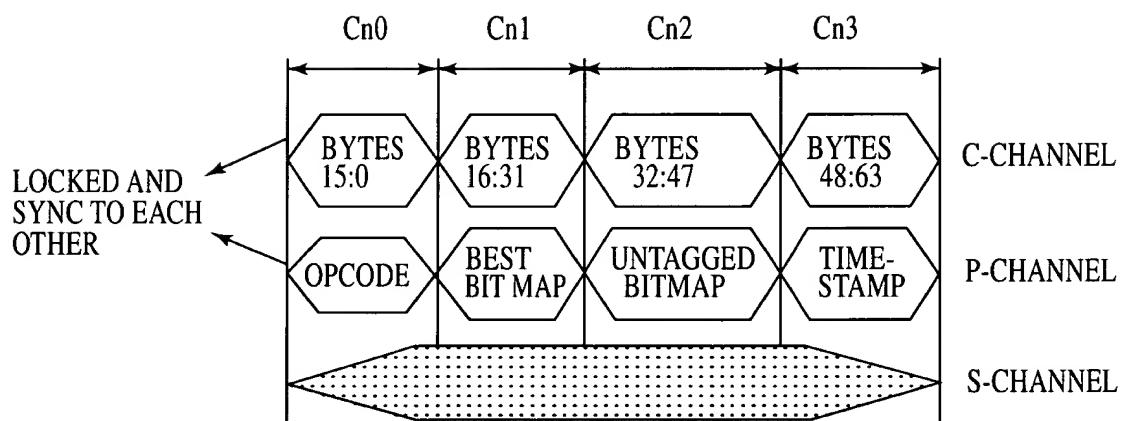


Fig.2



Fig.3



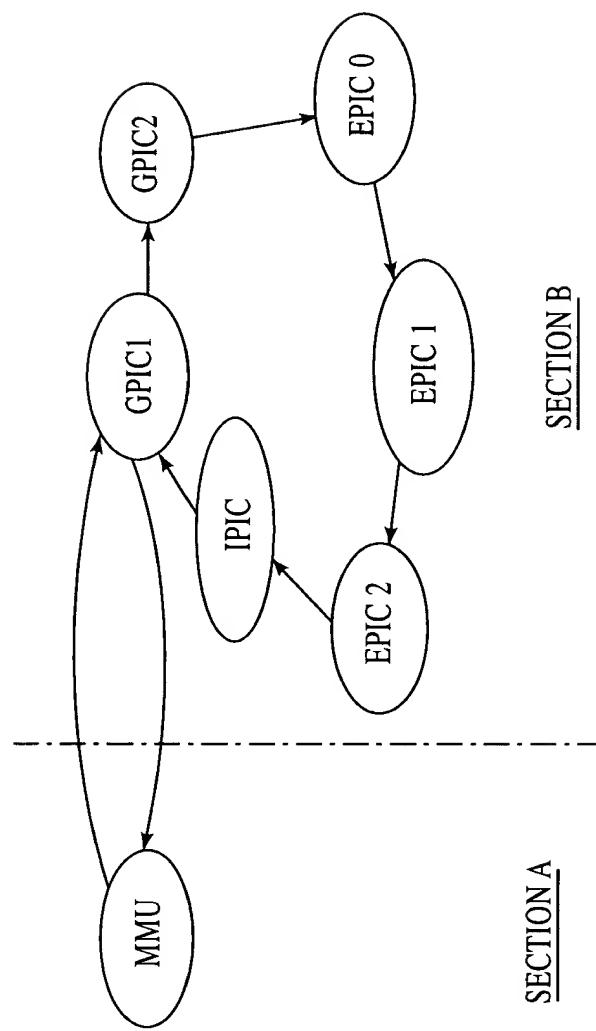


Fig. 4a

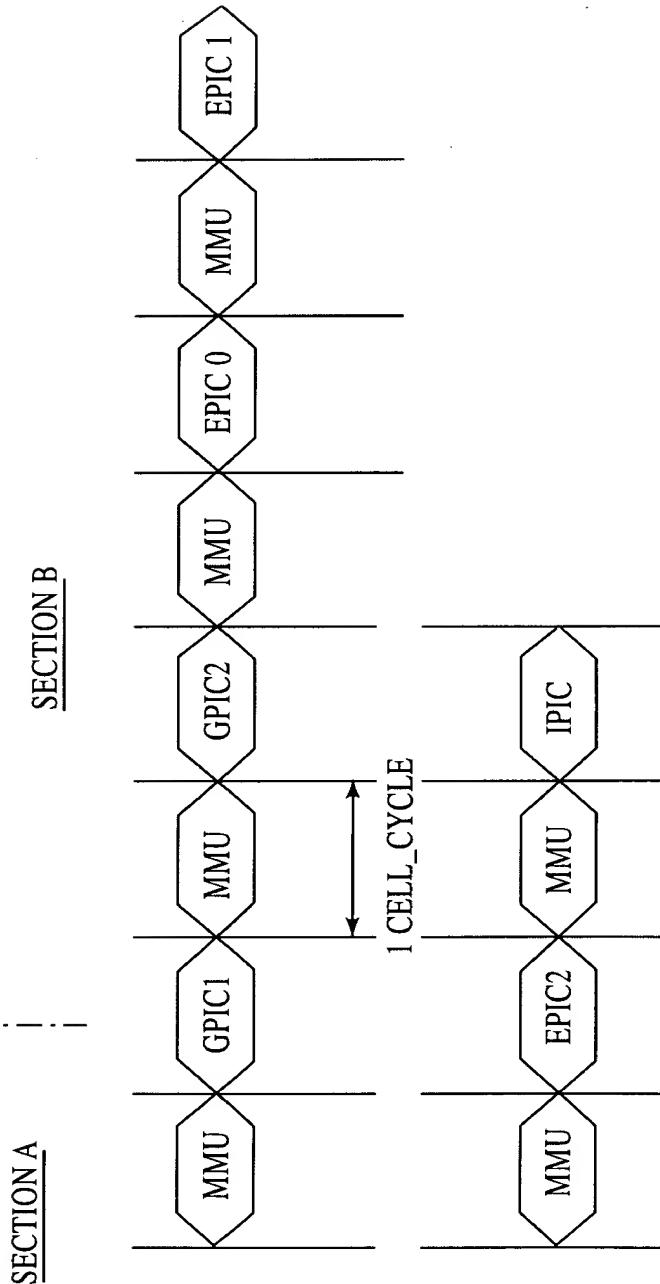


Fig. 4b



Fig.5

PROTOCOL CHANNEL MESSAGES

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
OPC ODE	IP IPX	RESE RVED	NXT CELL	SRC	DEST	PORT	COS	J	S	E	CRC	P	O	LEN	

R Bc / Mc PORTBITMAP

62	60	58	56	54	52	50	48	46	44	42	40	38	36	34	32
PF M	NEW IP CHECKSUM							M	MT-MODID			T	TGID	MOD OPCODE	c

U UNTAGGED PORTBITMAP / SRC PORT NUMBER (bit0..5)

62	60	58	56	54	52	50	48	46	44	42	40	38	36	34	32
RSVD	MATCHED FILTER	VLAN ID				SRC PORT				REMOTE PORT					

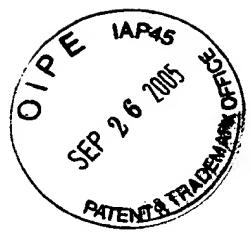
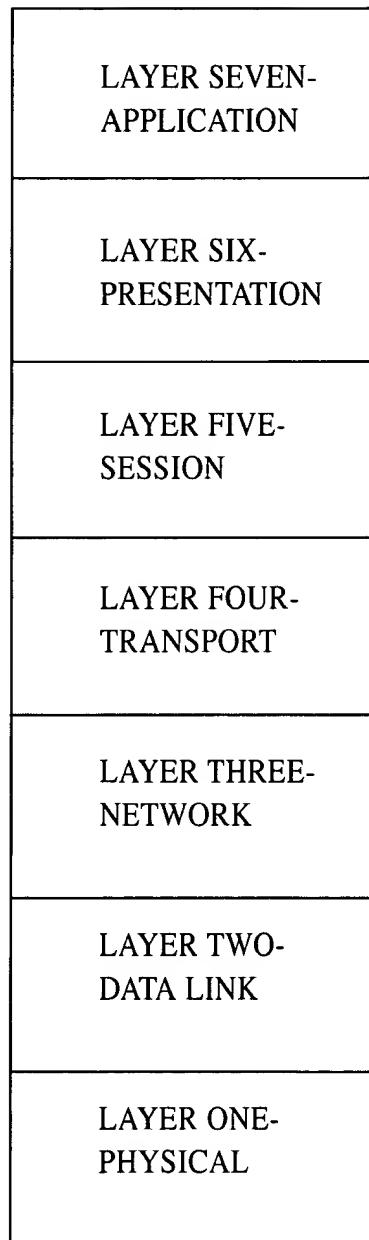


Fig.6

SIDE BAND CHANNEL MESSAGES



Fig.7
PRIOR ART



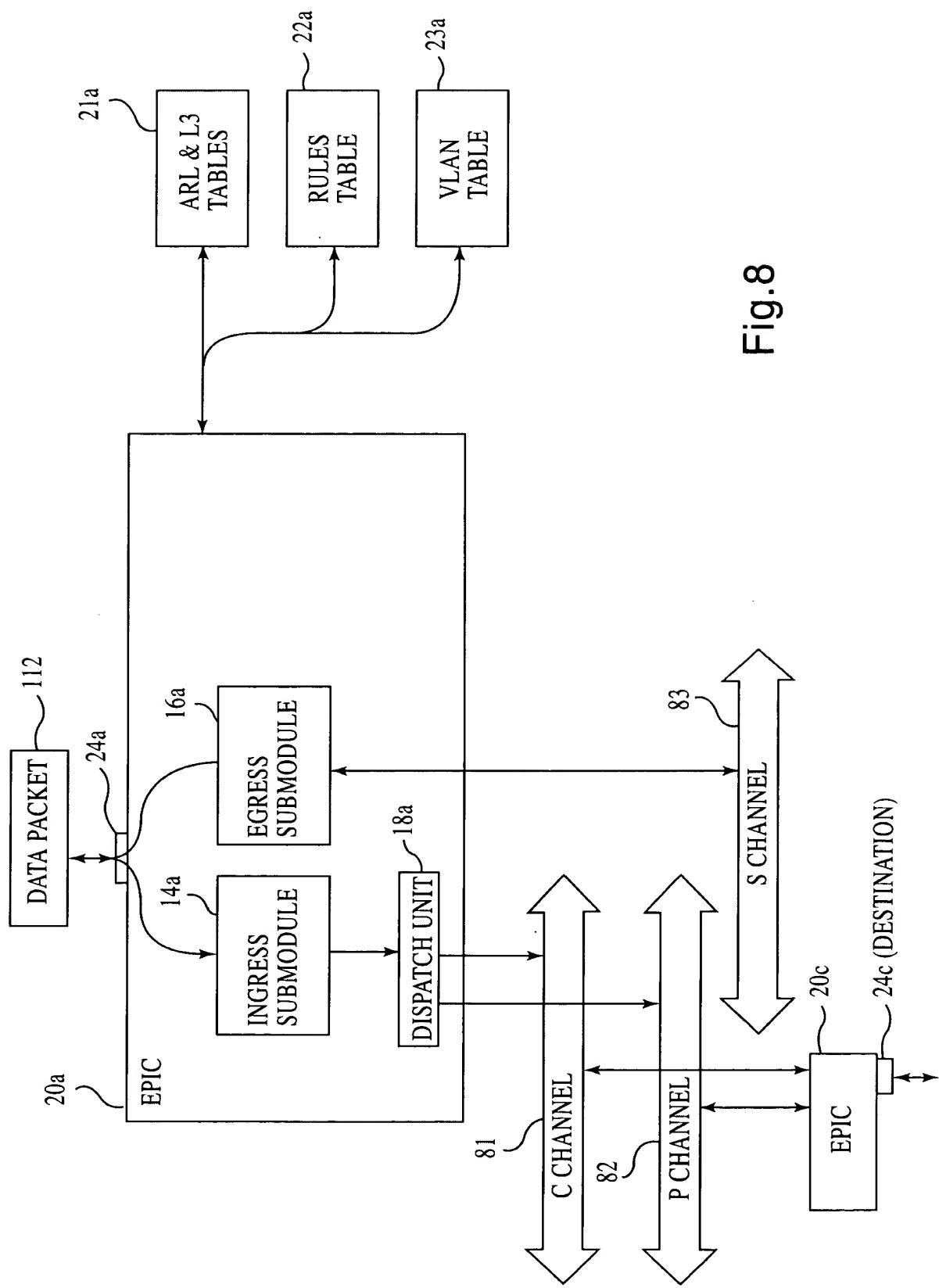




Fig.9

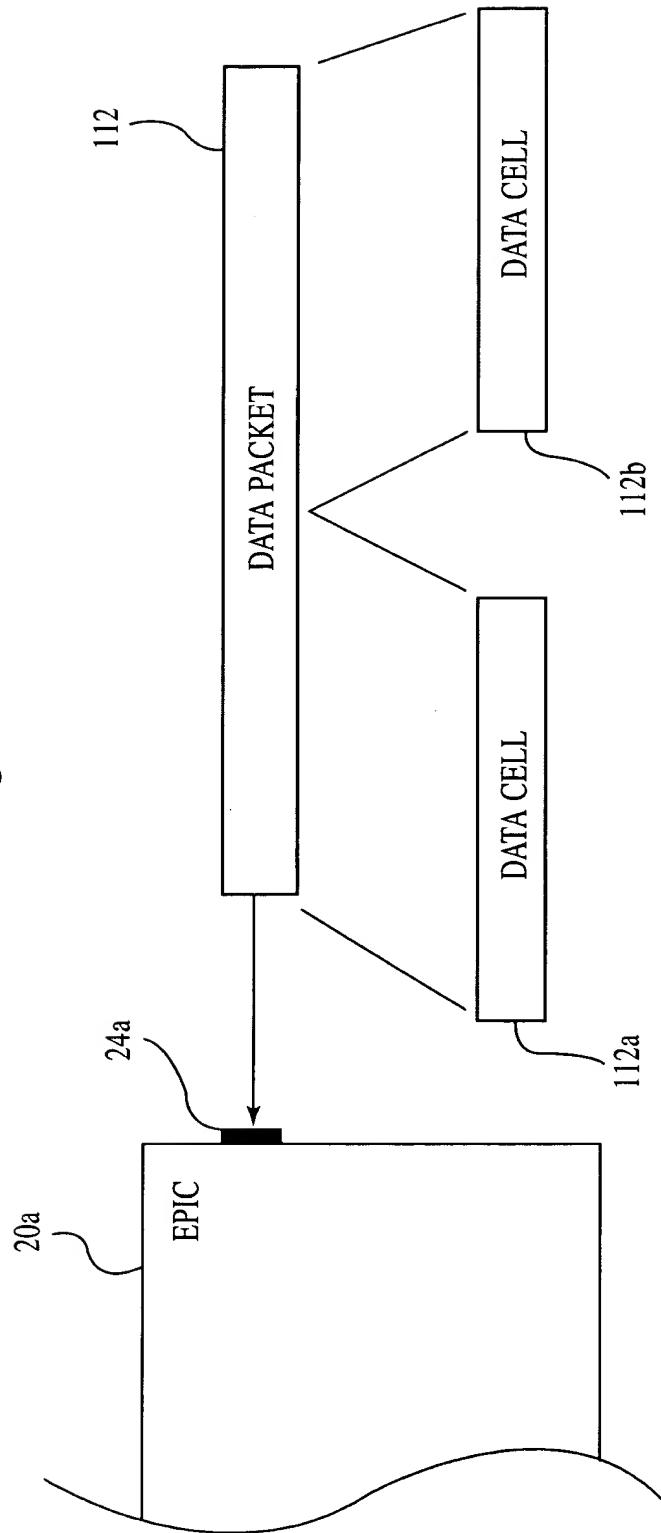




Fig.10

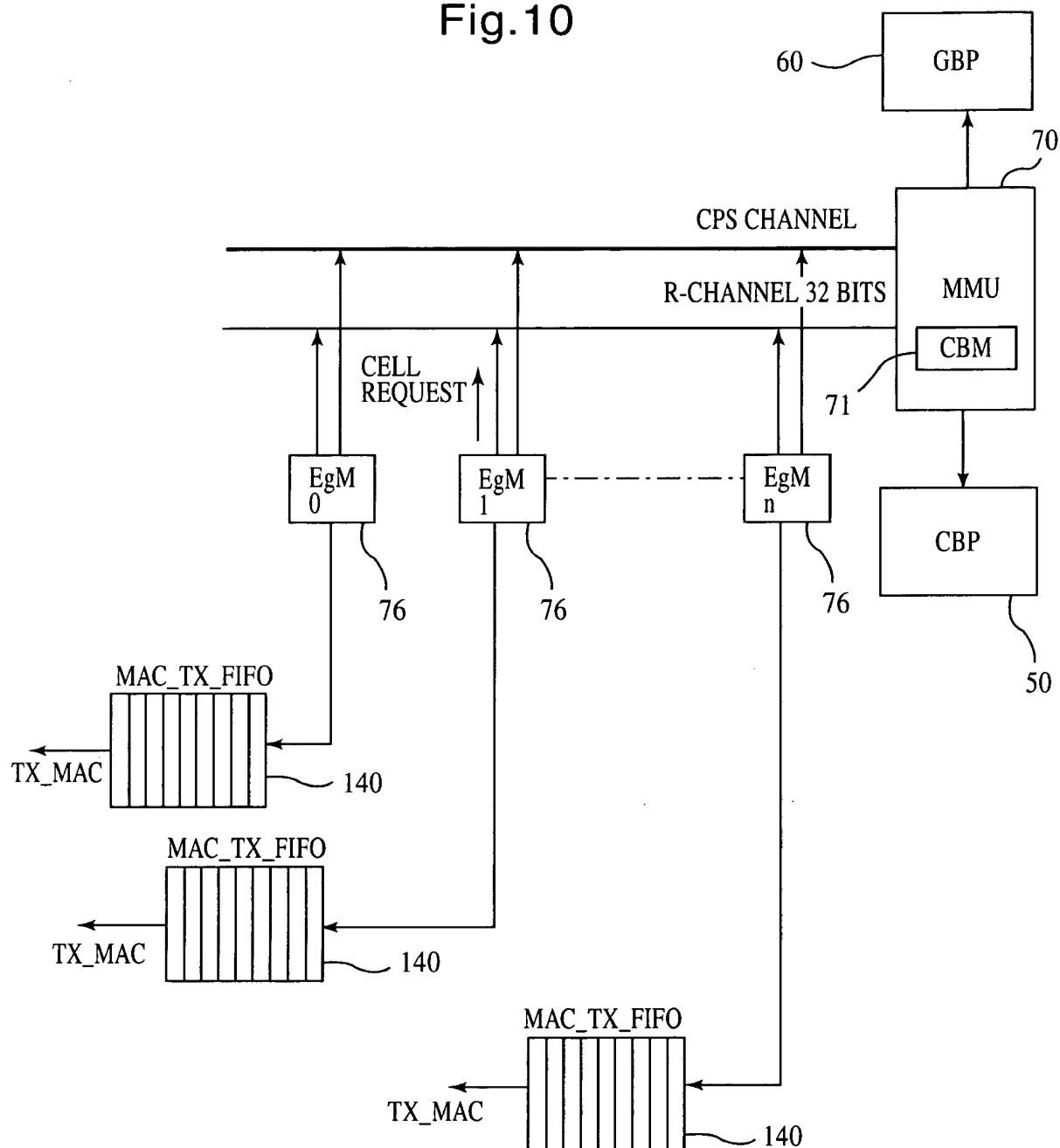




Fig. 11

LINE 0 →	FC LC BC/MC Cpy_cnt (5b) Cell_length (7b) CRC (2b) NC_header (16b) Src Count (6) IPX IP Time_Stamp (14b) O bits (2b) P NextCellLen(2b) CpuOpcode(4b) Cell_data (0-9B)
LINE 1 →	Cell_data (10-27) Bytes
LINE 2 →	Cell_data (28-45) Bytes
LINE 3 →	Cell_data (46-63) Bytes

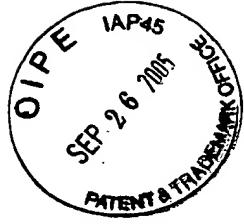


Fig.12

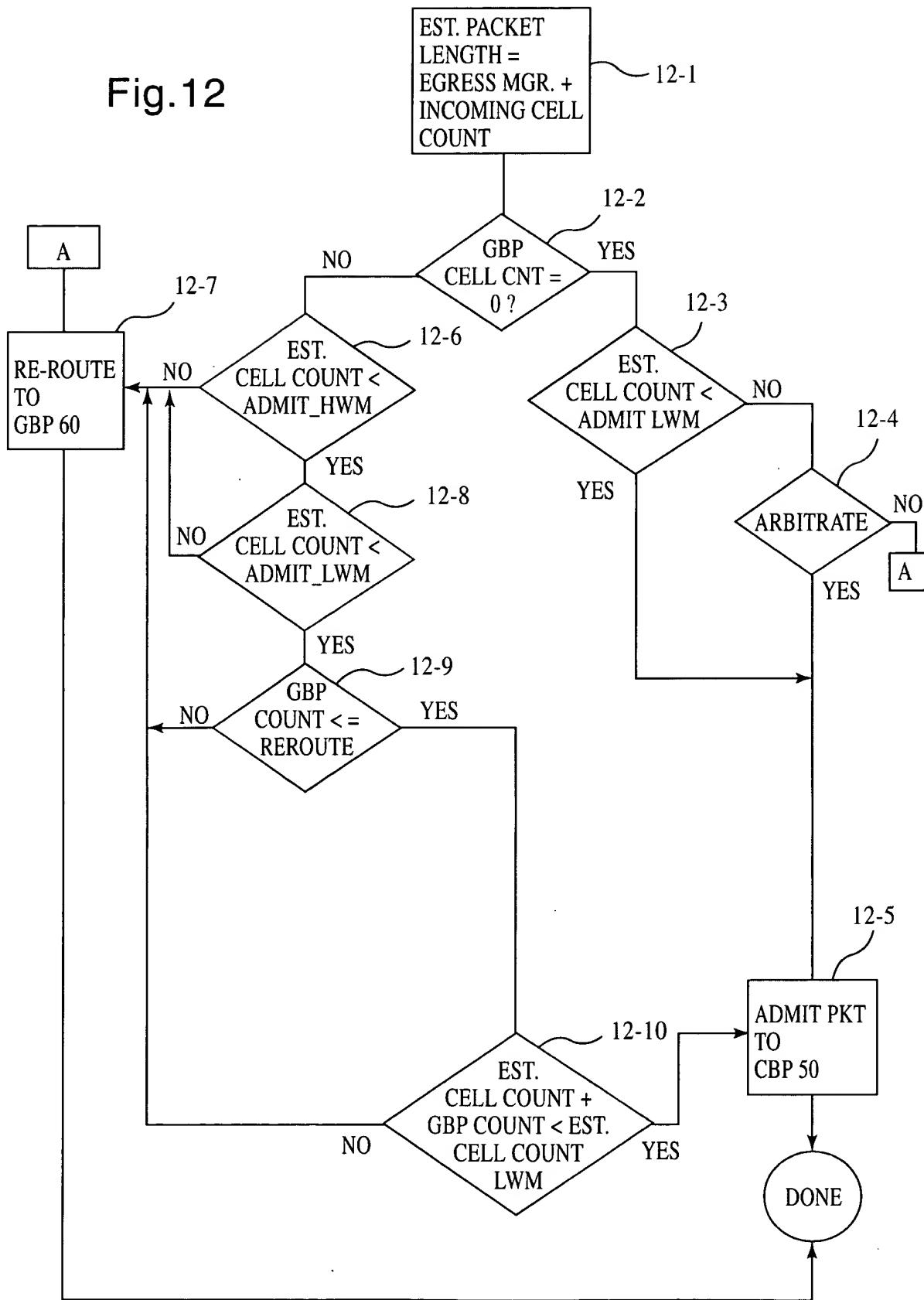




Fig.13

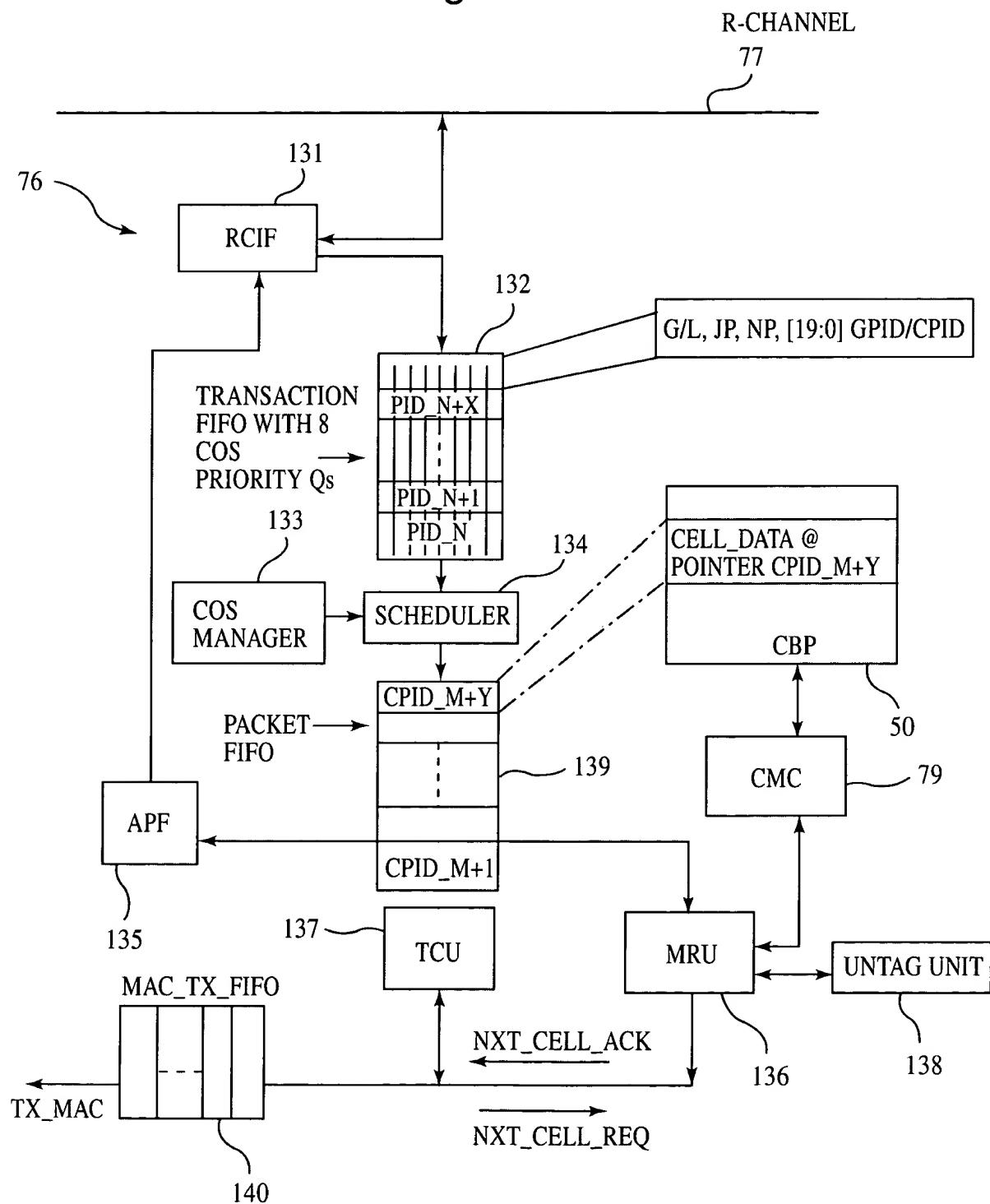


Fig.14

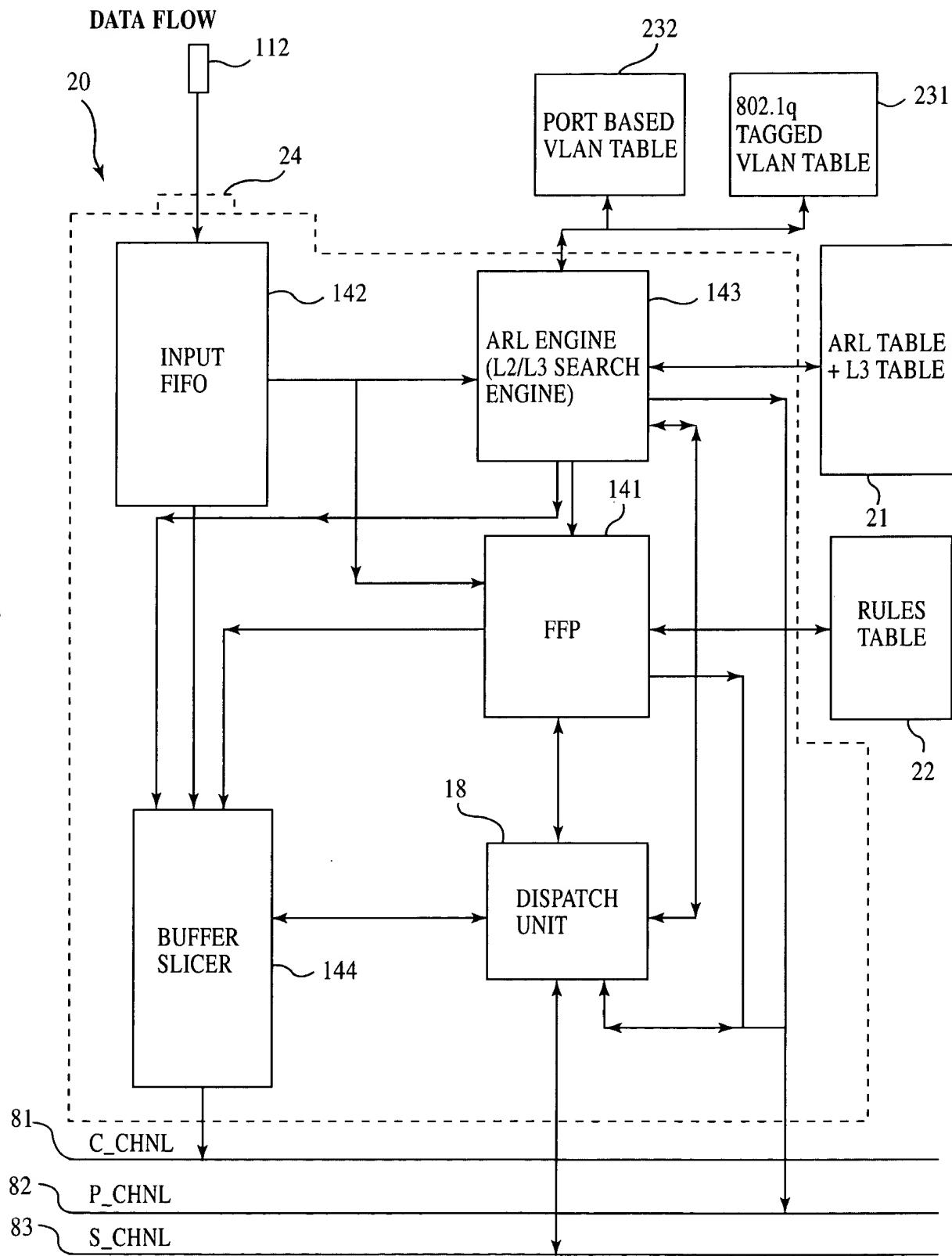
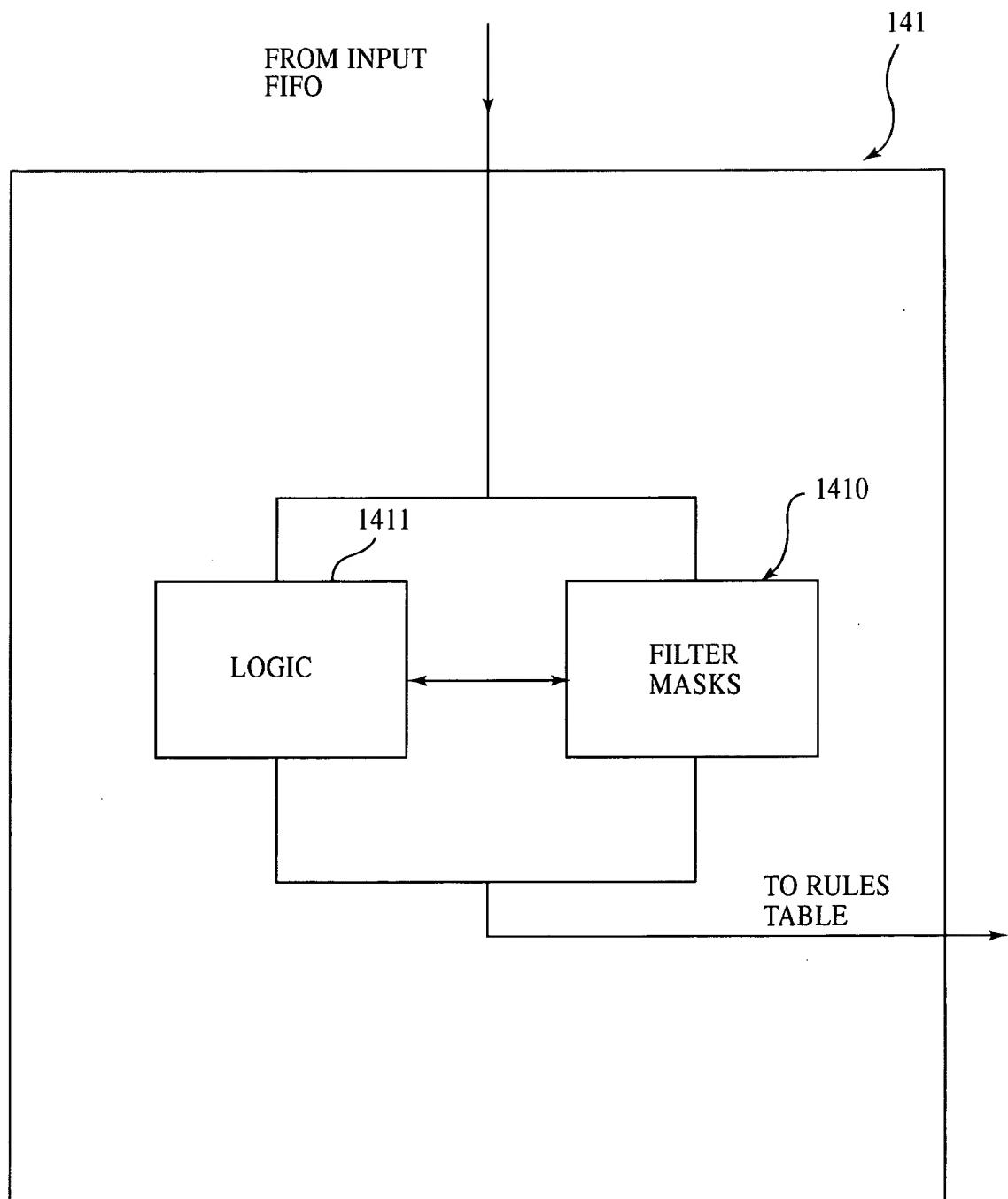




Fig.15



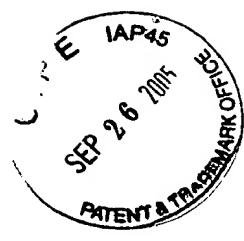


Fig.16

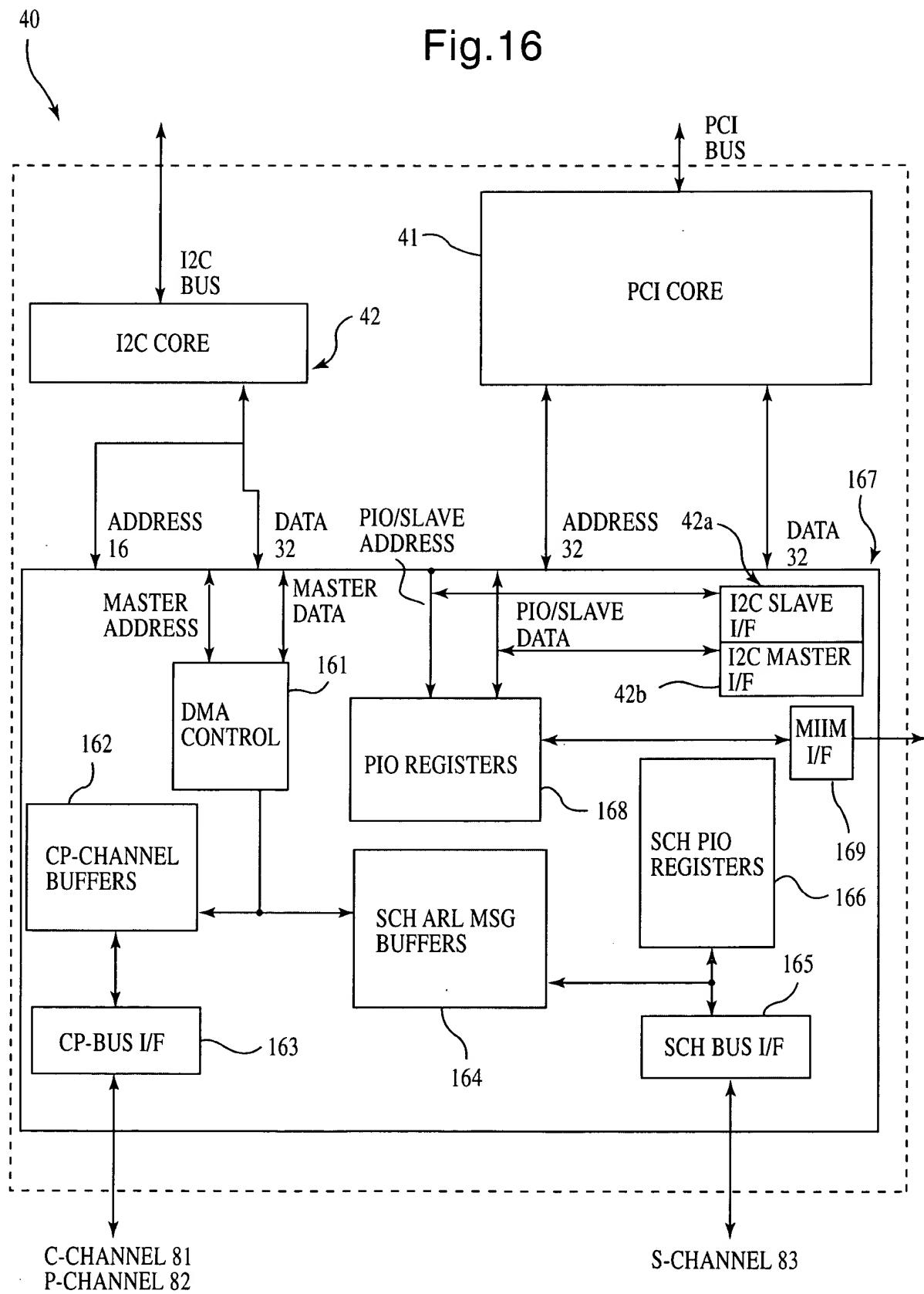
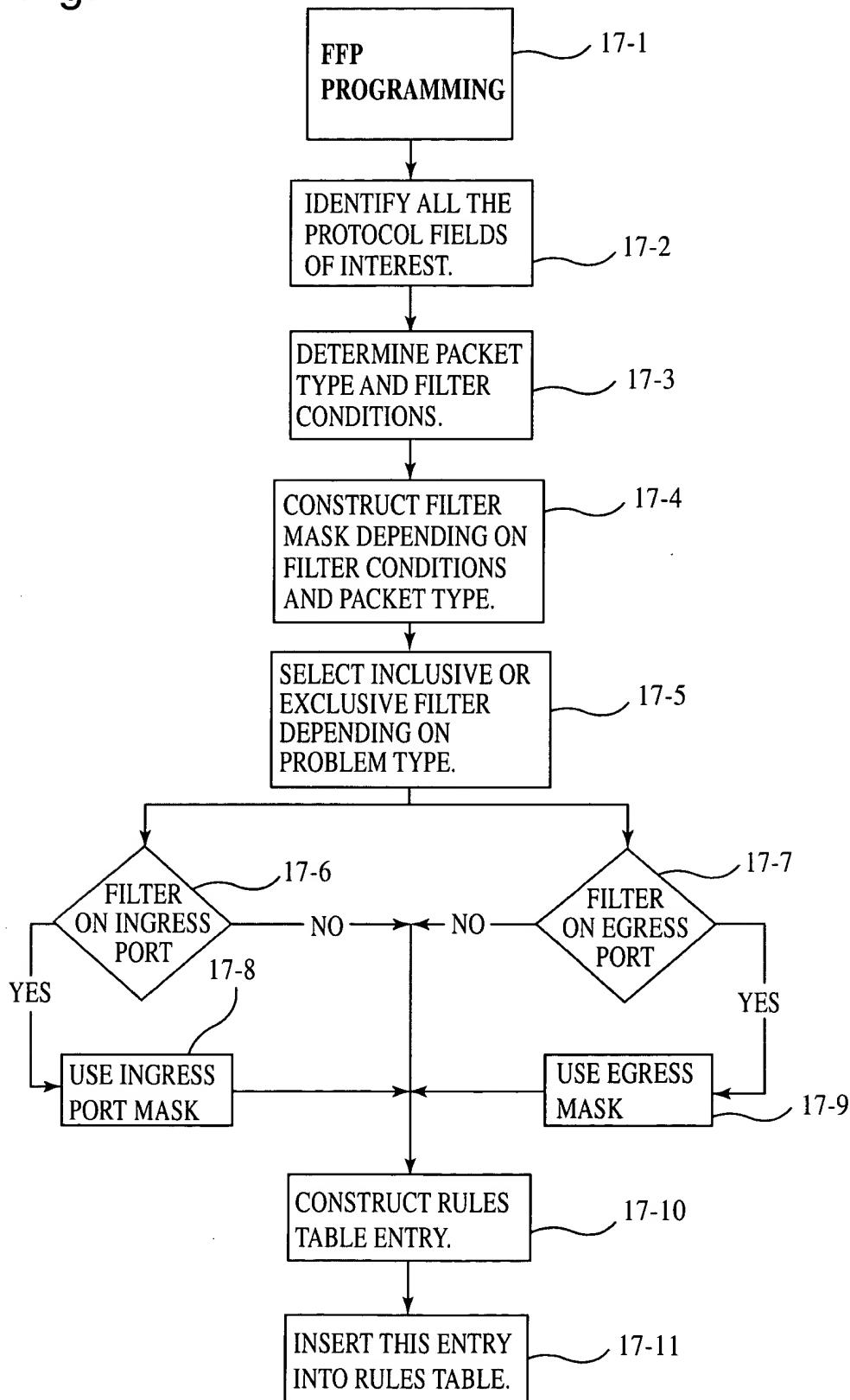
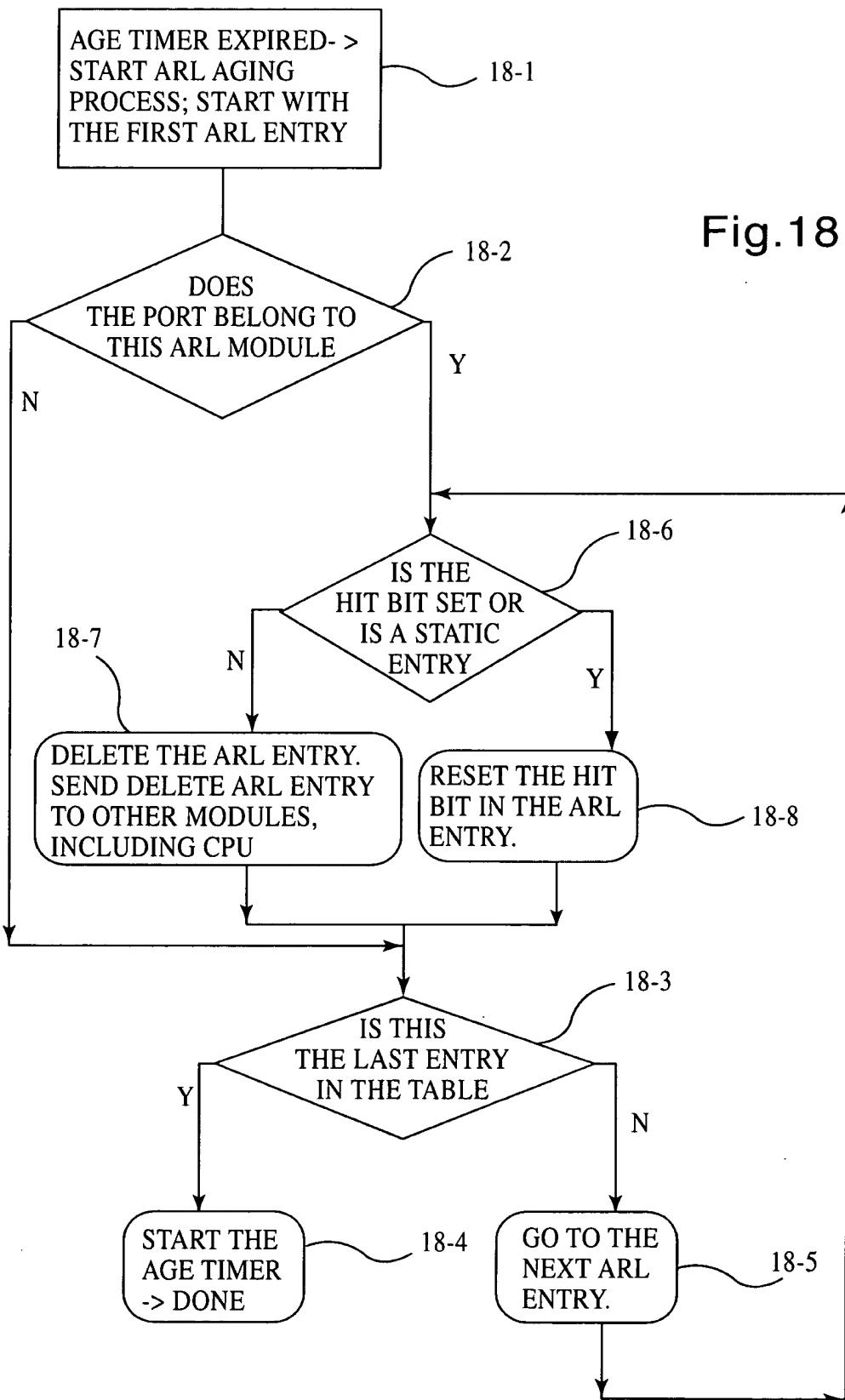




Fig.17

FFP PROGRAMMING FLOW CHART





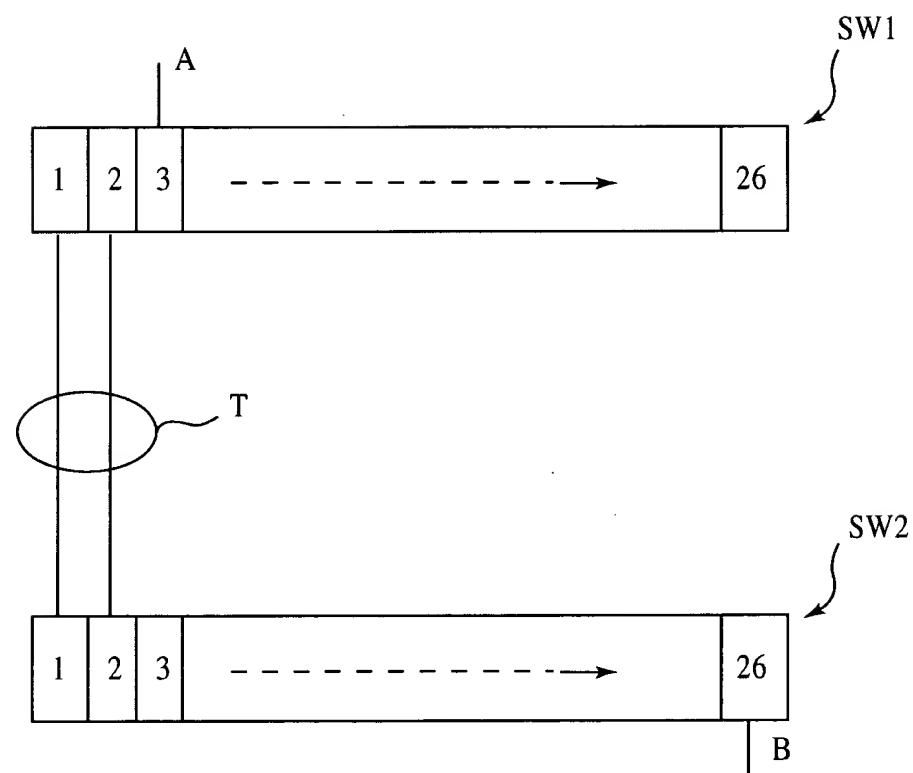


Fig.19



Fig.20

FIELD	HEADER	SIZE	OFFSET FOR ETHERNET II UNTAGGED	OFFSET FOR ETHERNET II TAGGED	OFFSET FOR SNAP UNTAGGED	OFFSET FOR SNAP TAGGED
DESTINATION MAC ADDRESS	MAC	6 BYTES	0	0	0	0
SOURCE MAC ADDRESS	MAC	6 BYTES	6	6	6	6
PROTOCOL TYPE	MAC	2 BYTES	12	16	20	24
DESTINATION TYPE	802.3	1 BYTE	NA	NA	14	18
SOURCE SAP	802.3	1 BYTE	NA	NA	15	19
802.1p PRIORITY	MAC	3 BITS	NA	14	NA	14
VLAN Id	MAC	12 BITS	NA	14+4b	NA	14+4b
TOS PRECEDENCE	IP	3 BITS	15	19	23	27
DIFFERENTIATED SERVICES	IP	6 BITS	15	19	23	27
SOURCE IP ADDRESS	IP	4 BYTES	26	30	34	38
DESTINATION IP ADDRESS	IP	4 BYTES	30	34	38	42
PROTOCOL	IP	1 BYTE	23	27	31	35
SOURCE PORT	TCP/UDP	2 BYTES	34	38	42	46
DESTINATION PORT	TCP/UDP	2 BYTES	36	40	44	48
TCP CONTROL FLAGS (FOR ALIGNING ON BYTE BOUNDARY 2 BITS OF RESERVED BITS PRECEDING THIS FIELD IS INCLUDED)	TCP	1 BYTE	47	51	55	59
DATA AT OFFSET 1	NA	8 BYTES	DATA OFFSET1 FROM START OF IP/IPX HEADER			
DATA AT OFFSET 2	NA	8 BYTES	DATA OFFSET2 FROM START OF IP/IPX HEADER			
DATA AT OFFSET 3	NA	8 BYTES	DATA OFFSET3 FROM START OF IP/IPX HEADER			
DATA AT OFFSET 4	NA	8 BYTES	DATA OFFSET4 FROM START OF IP/IPX HEADER			



Filter Mask Format:

Filter Enable (1b)	Counter (5b)	Rem Port (1b)	Output Mod (5b)	Output Port (6b)	TOS Prec (3b)	Diff Serv (6b)	802.1p Prior (3b)
NMA Enb (1b)	No Match Action (10b)	Data Offset 4 (7b)	Data Offset 3 (7b)	Data Offset 2 (7b)	Data Offset 1 (7b)	Ingress Port Mask (6b)	Egress ModId Mask (5b)
Field Mask							

Fig.21a

Field Mask Format:

Dest Mac addr (6B)	Src Mac addr (6B)	Prot type (2B)	Dest SAP (1B)	Src SAP (1B)	802.1 p Prio (3b)	Vlan Id (12b)	TOS Prec (3b)	Diff Serv (6b)	Src IP addr (4B)	Dest IP addr (4B)	Prot IP- (1B)	Src Port (2B)	Dest Port (2B)
TCP Cntr Flags (1B)		Data 1 (8B)		Data 2 (8B)		Data 3 (8B)		Data 4 (8B)					

Fig.21b

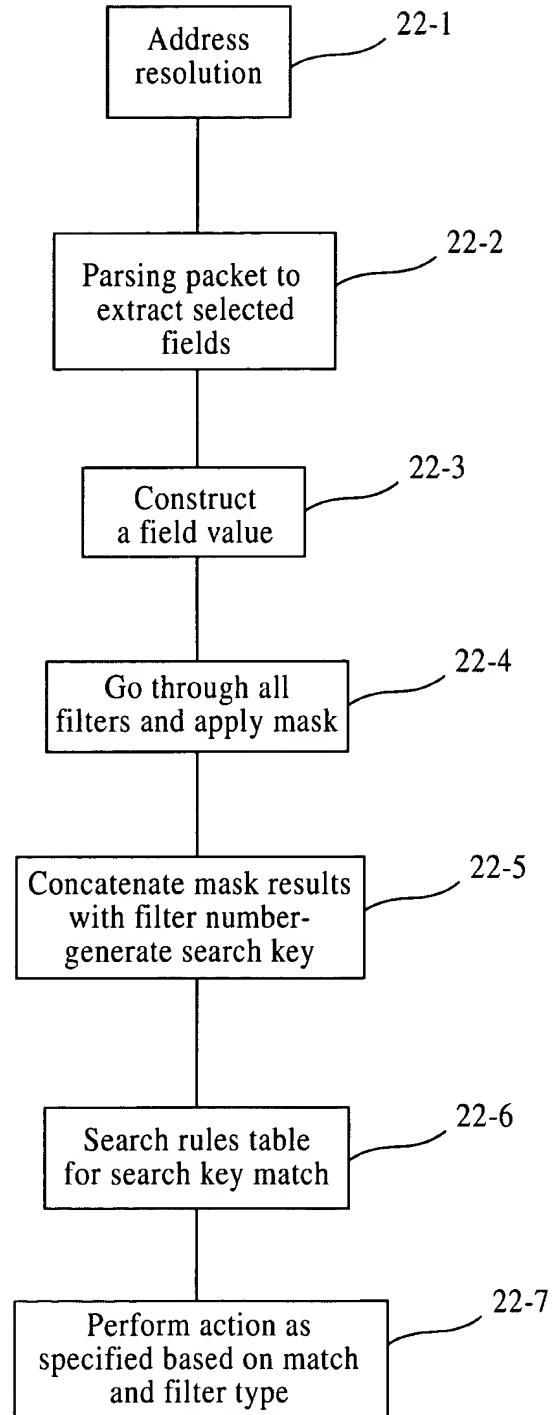
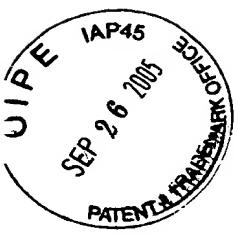


Fig.22



Count er (5b)	Output Mod (5b)	Output Port (6b)	TOS_ P (3b)	Diff Services (6b)	802.1p Priority (3b)	Action (11b)	Filter Select (3b)	Ingress Port (6b)	Egrs Mod (5b)	Egrs Port (6b)	Filter Value (512b)

22

Fig.23



30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
Source IP Address															
Multicast IP Address															
L3 Port Bitmap															
L3 Module Bitmap															
Unused										TTL Threshold		Source Port			

Fig.24

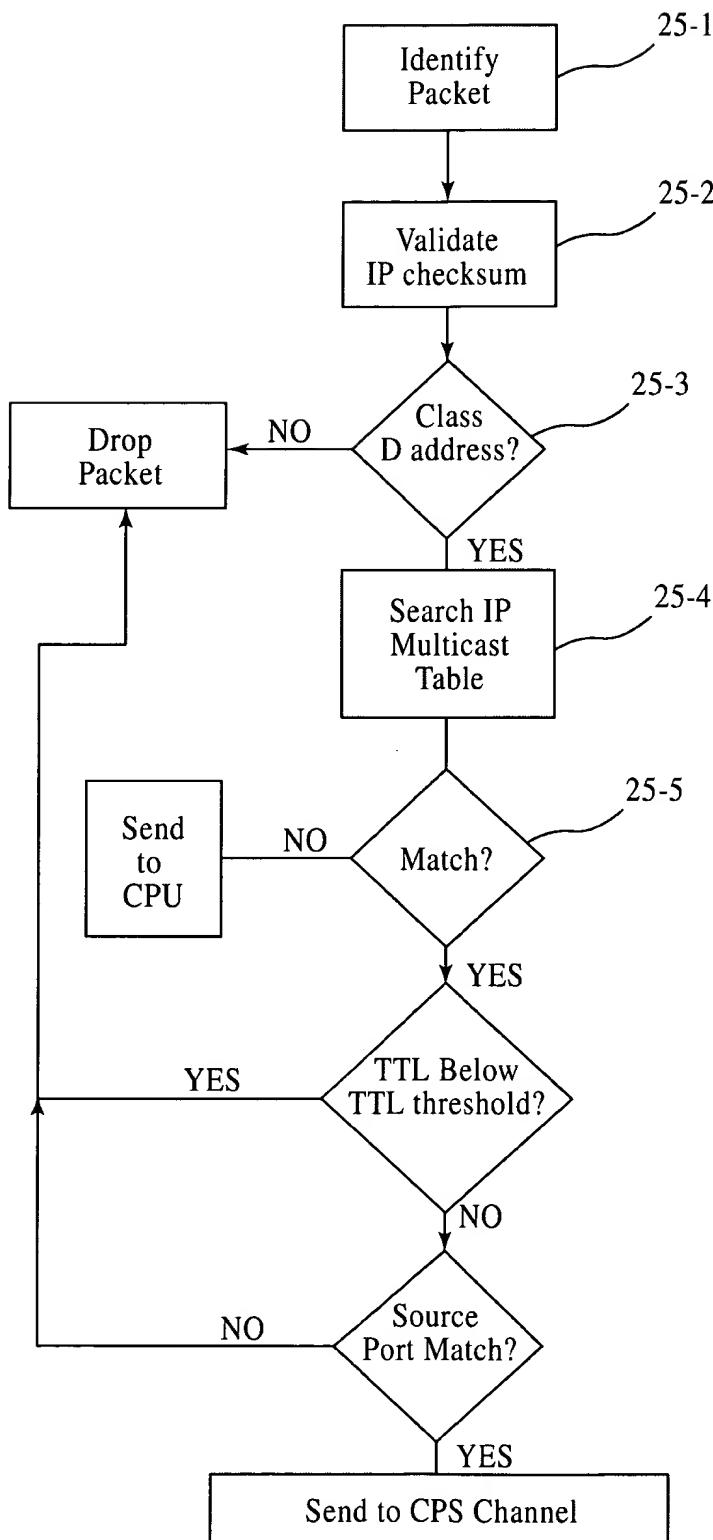


Fig.25

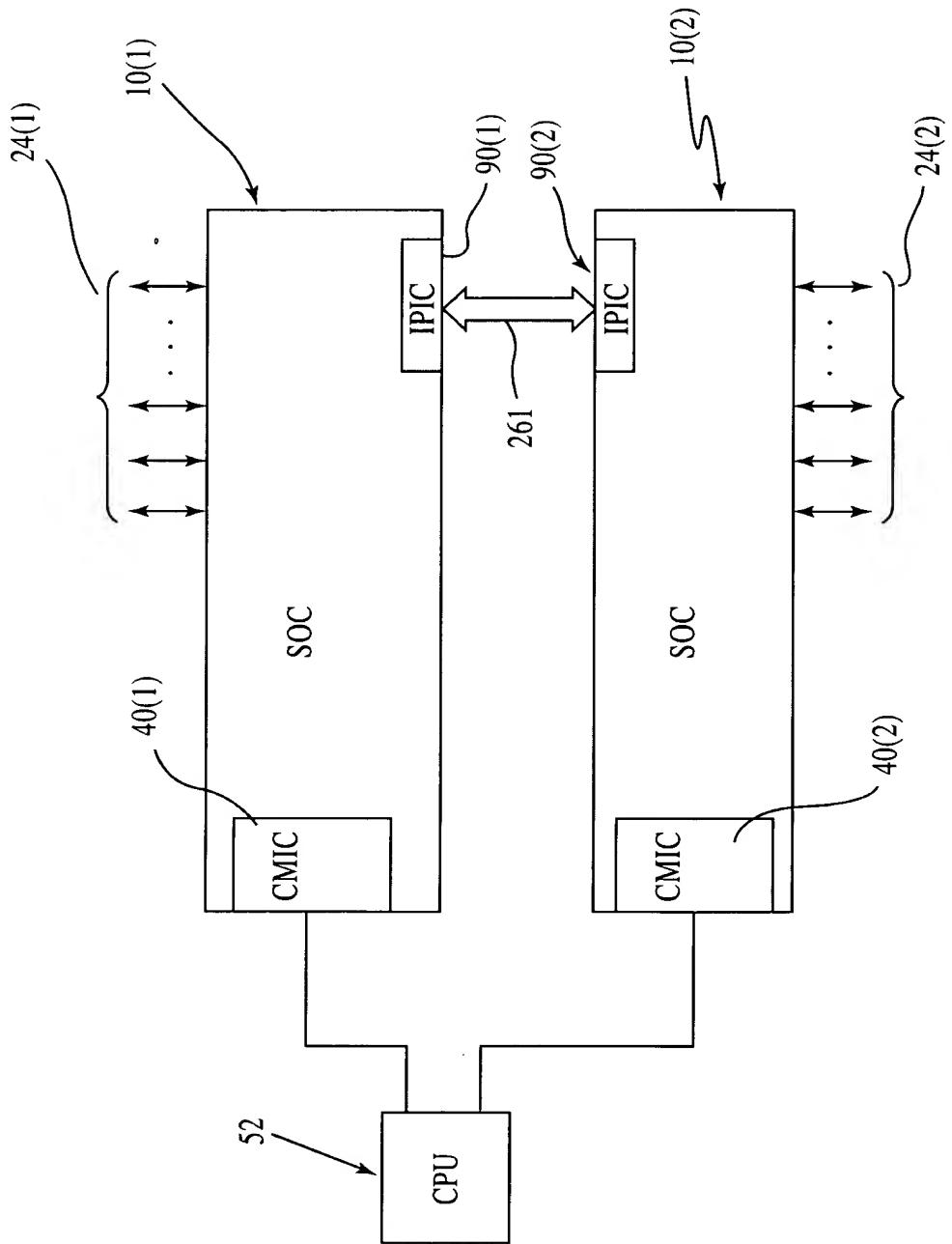


Fig.26



Fig.27a

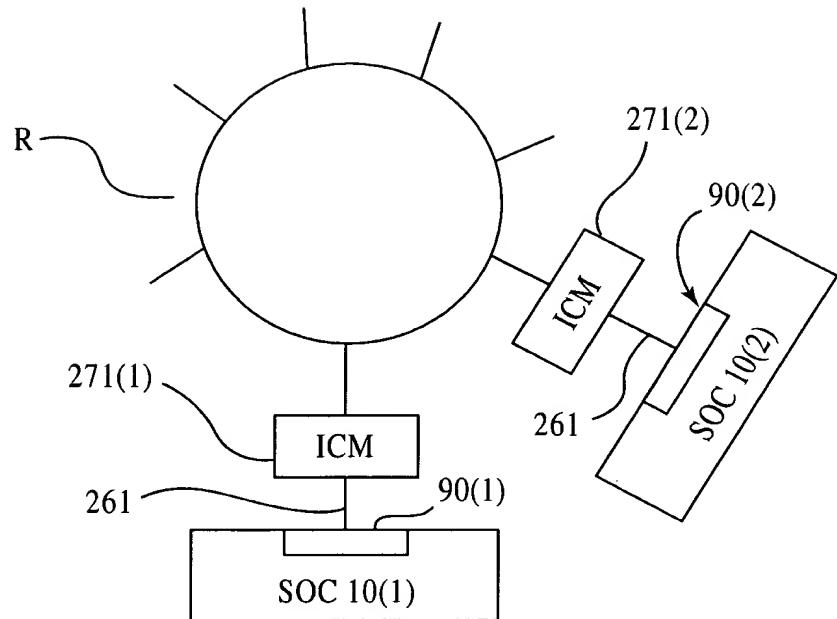
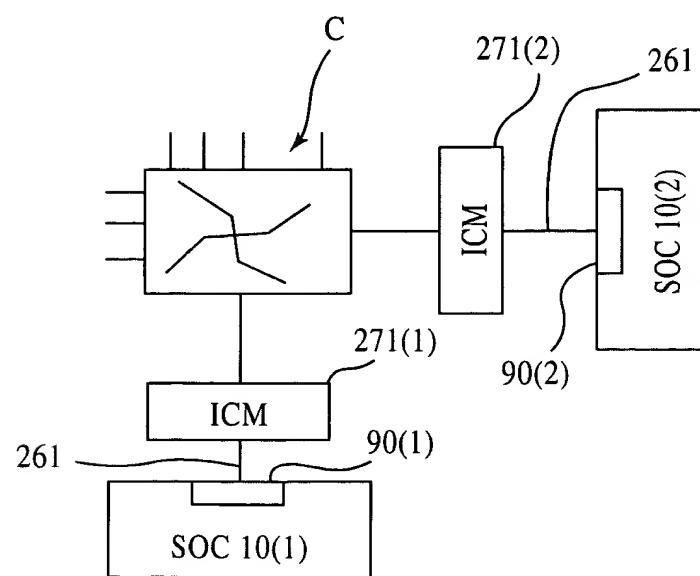


Fig.27b



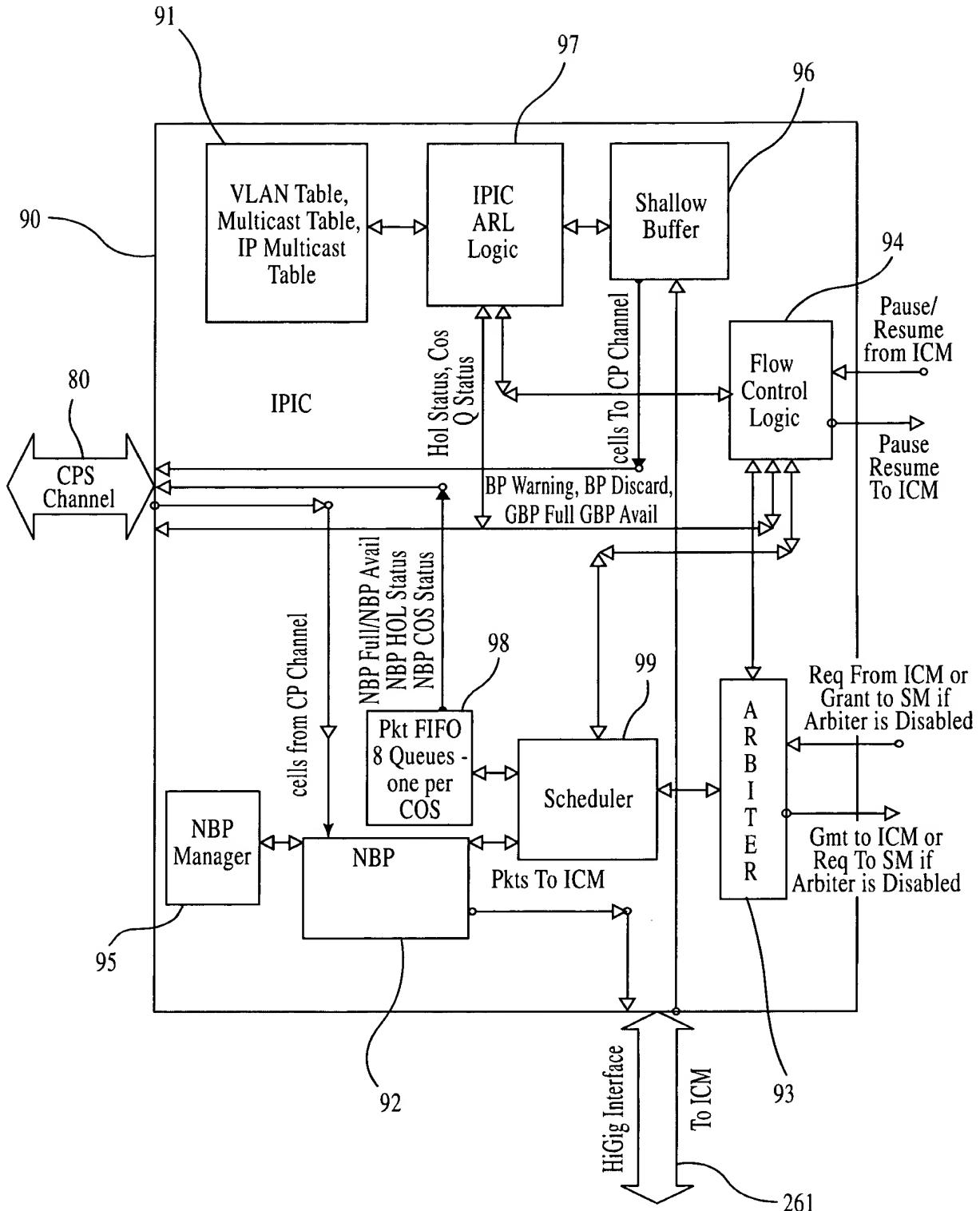
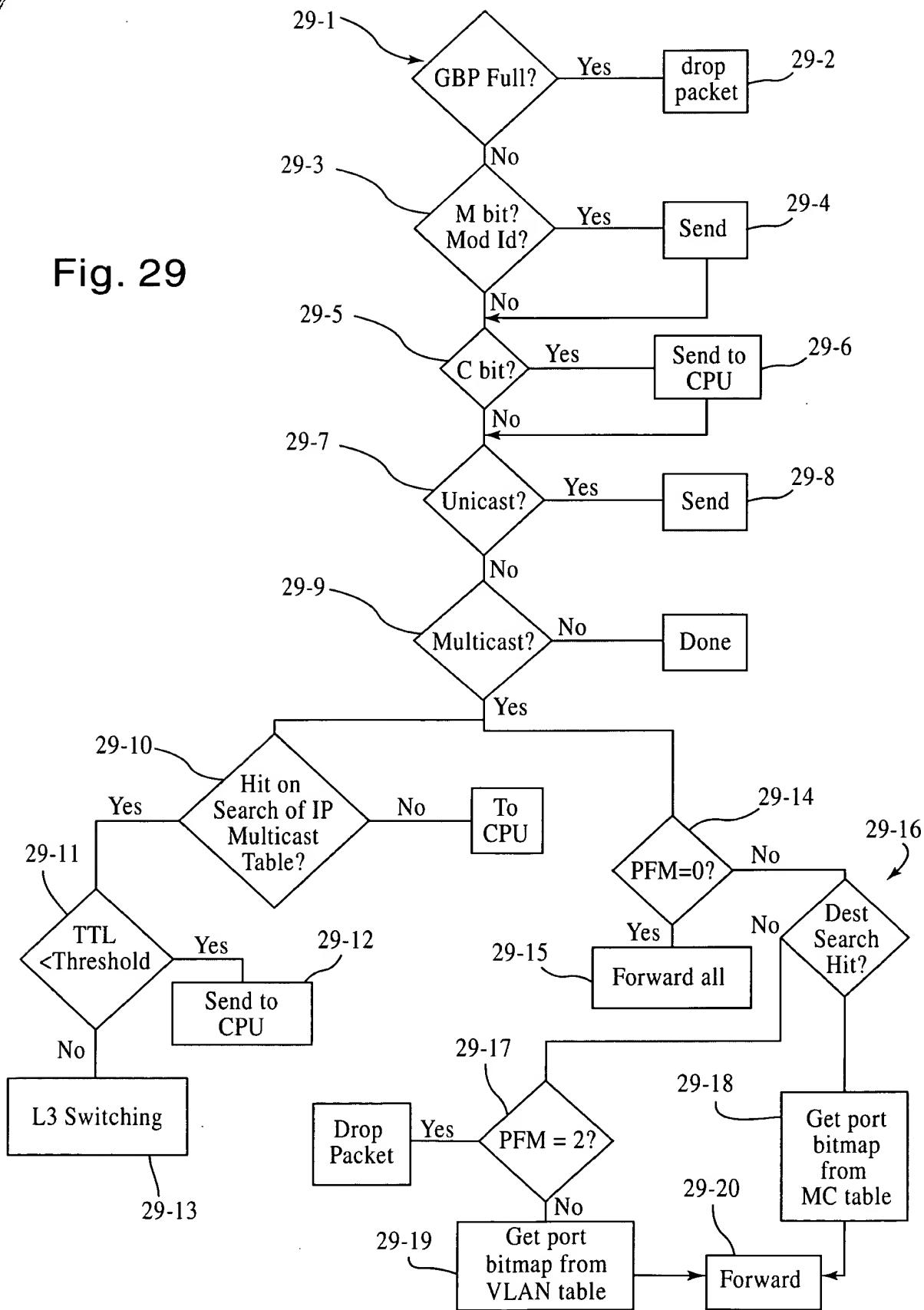


Fig.28

Fig. 29





COS Queue (3b)	C P F	NCA (2b)	802.1p Priority (3b)	Rate Counter (8b)	Rate Counter Threshold (8b)	Rate Discard Threhold (8b)	New Code Point (6b)	New COS Queue (3b)	New 802.1 Priority (3b)
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Fig.30



Offset Field	Offset 1	Offset 2	Offset 3	Offset 4
000	0-15	16-31	32-47	48-63
001	8-23	24-39	40-55	56-71
010	16-31	32-47	48-63	64-79
011	24-39	40-55	56-71	72-87
100	32-47	48-63	64-79	80-95
101	40-55	56-71	72-87	88-103
110	48-63	64-79	80-95	96-111
111	56-71	72-87	88-103	104-119

Fig.31

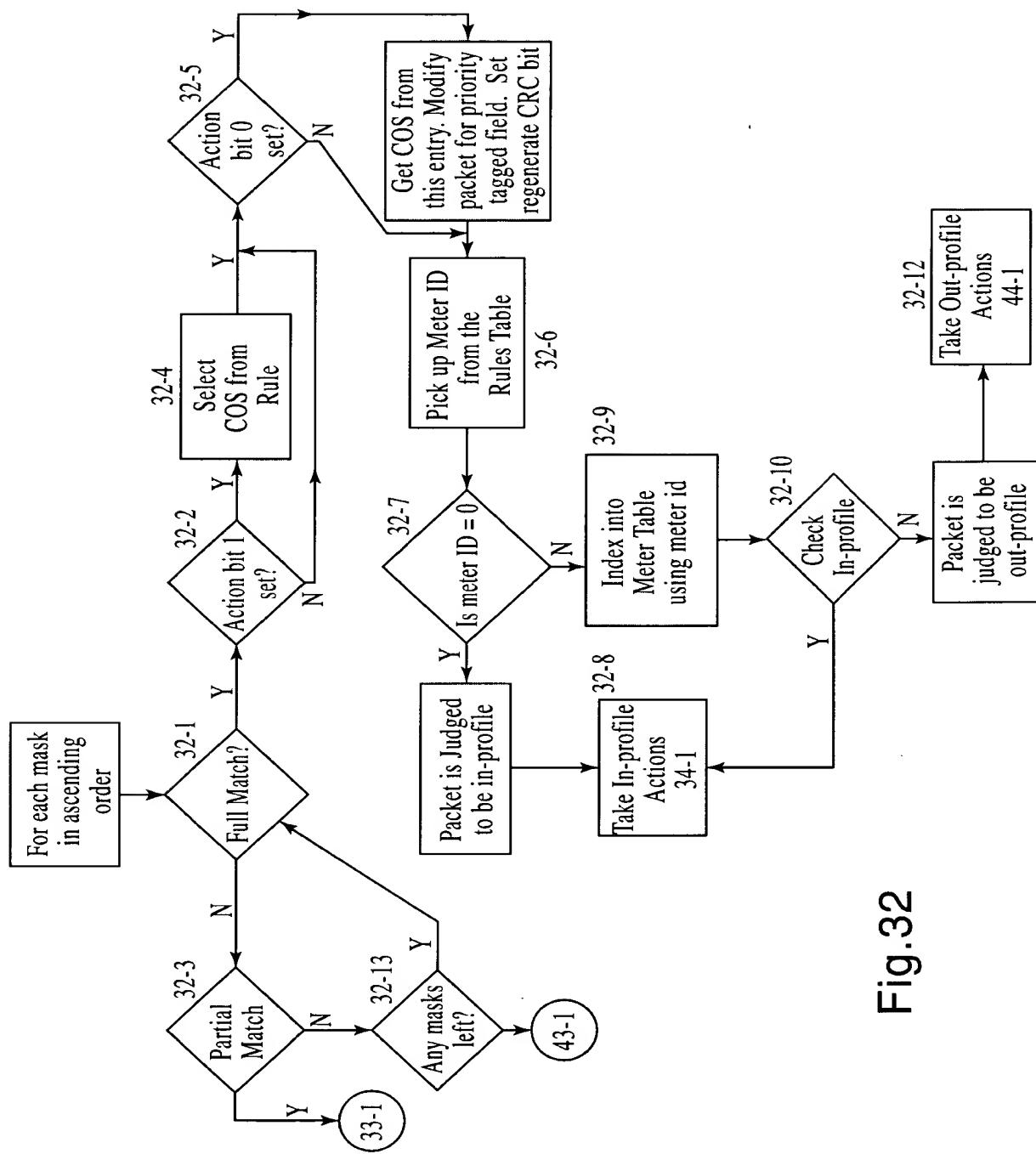


Fig.32

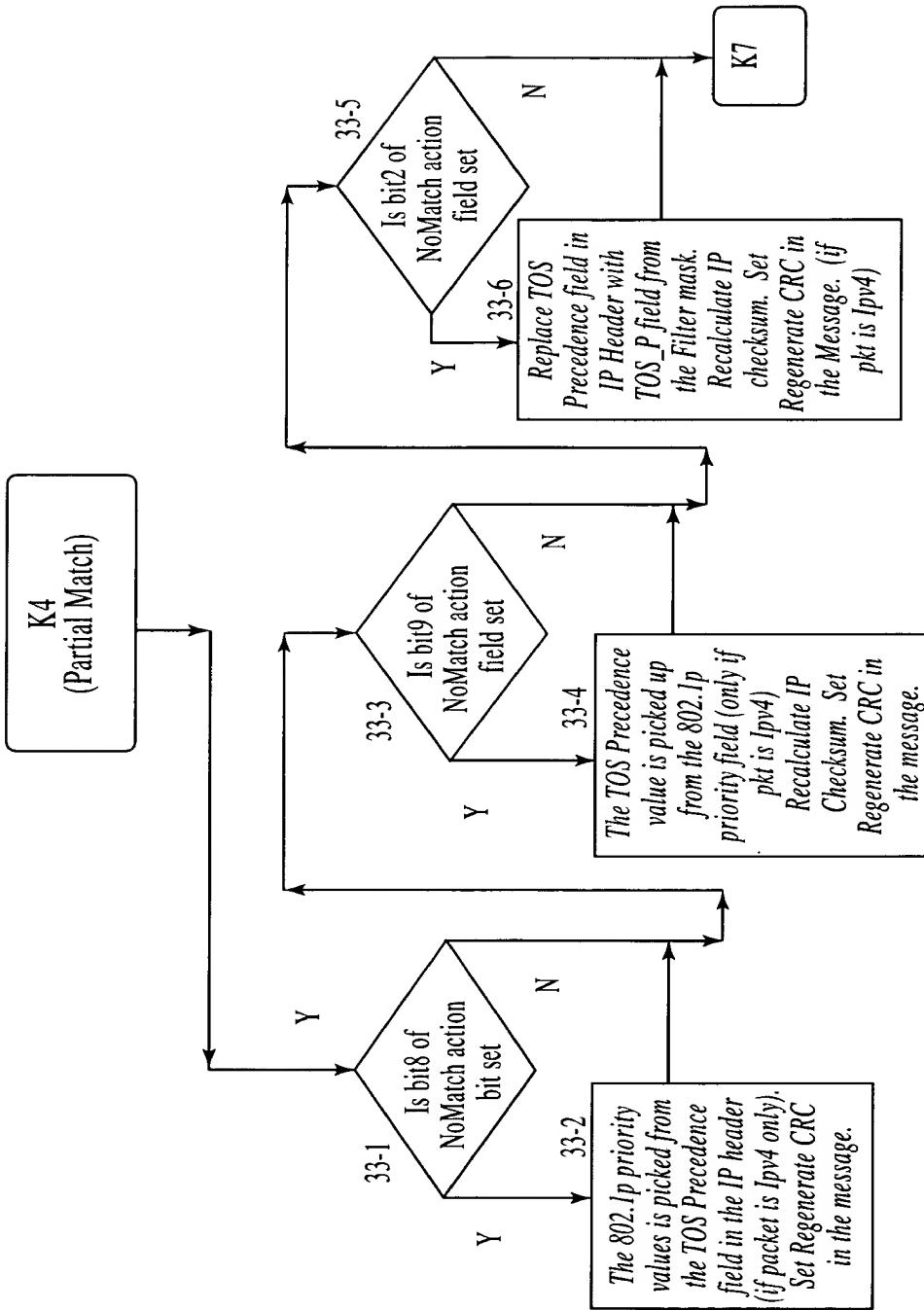


Fig. 33

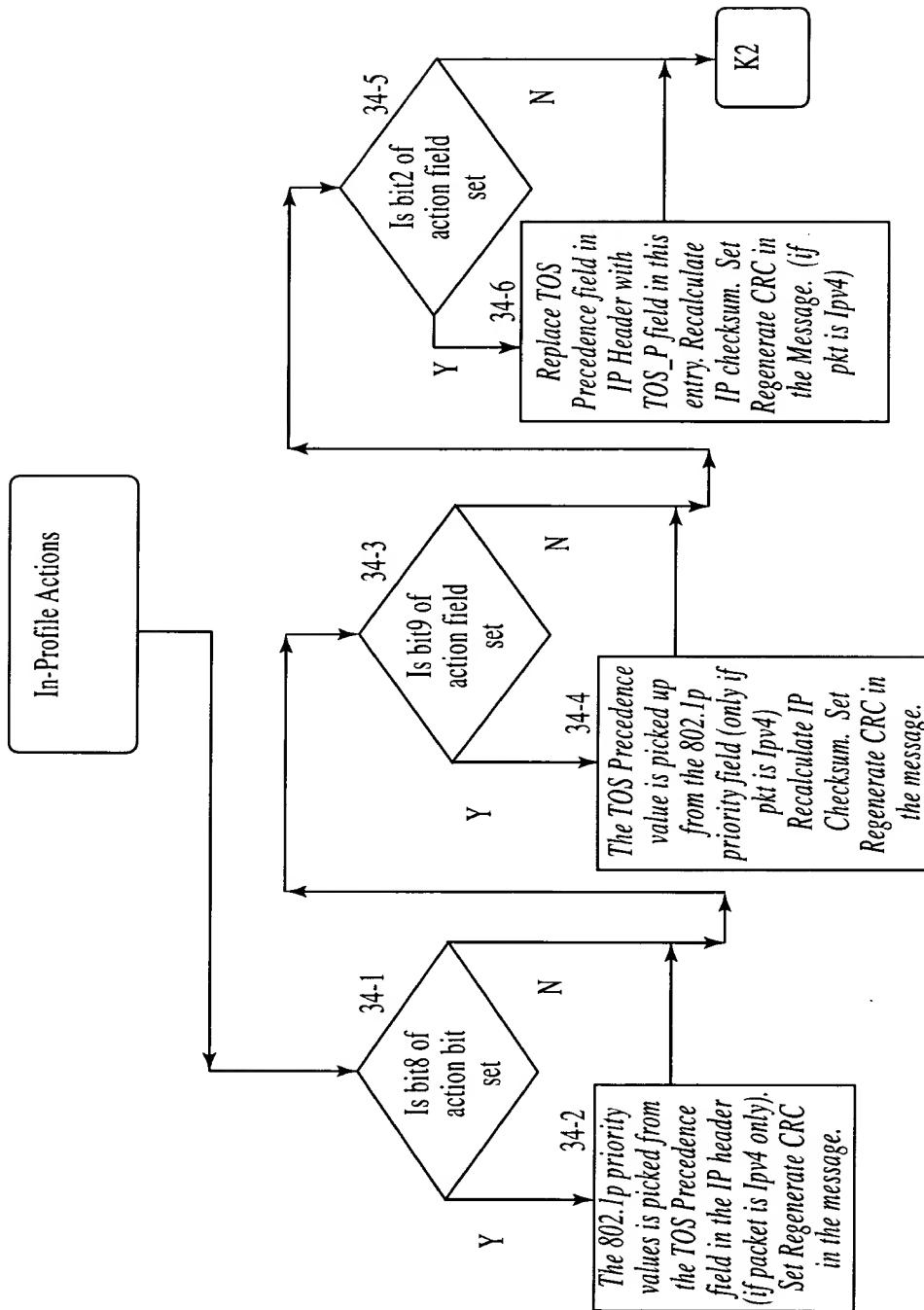
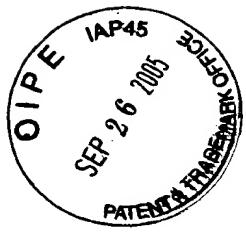


Fig. 34

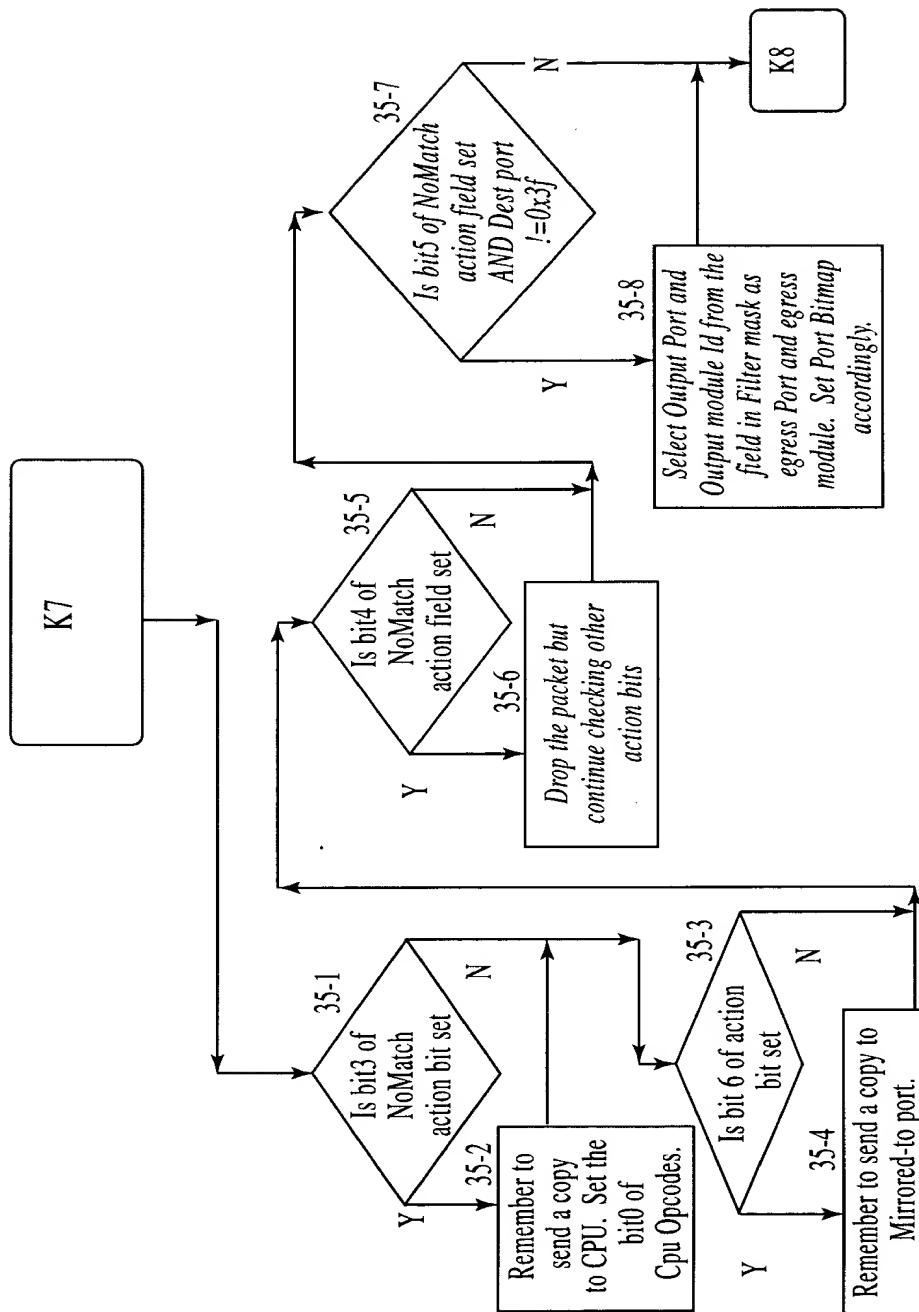


Fig.35

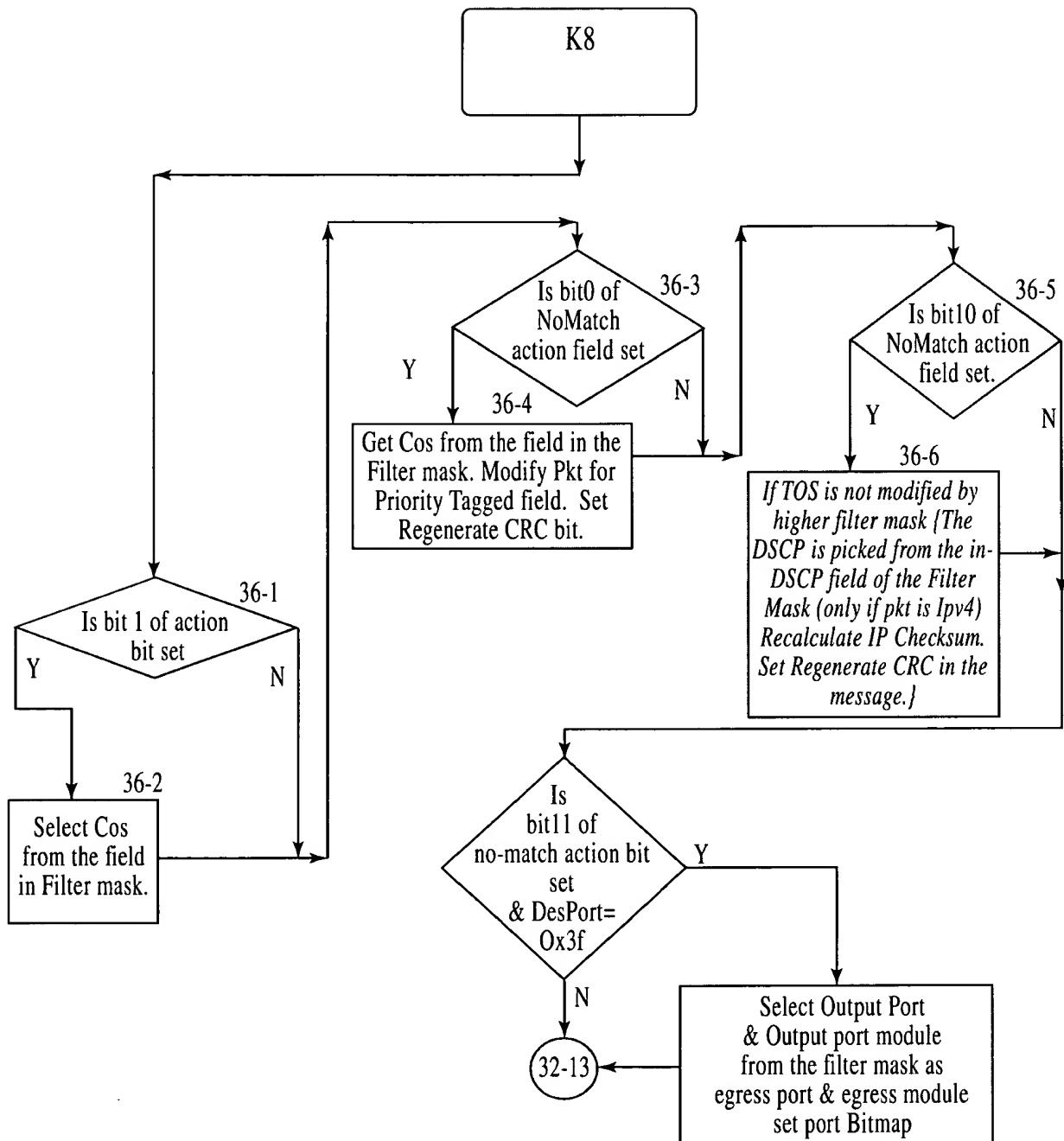


Fig.36

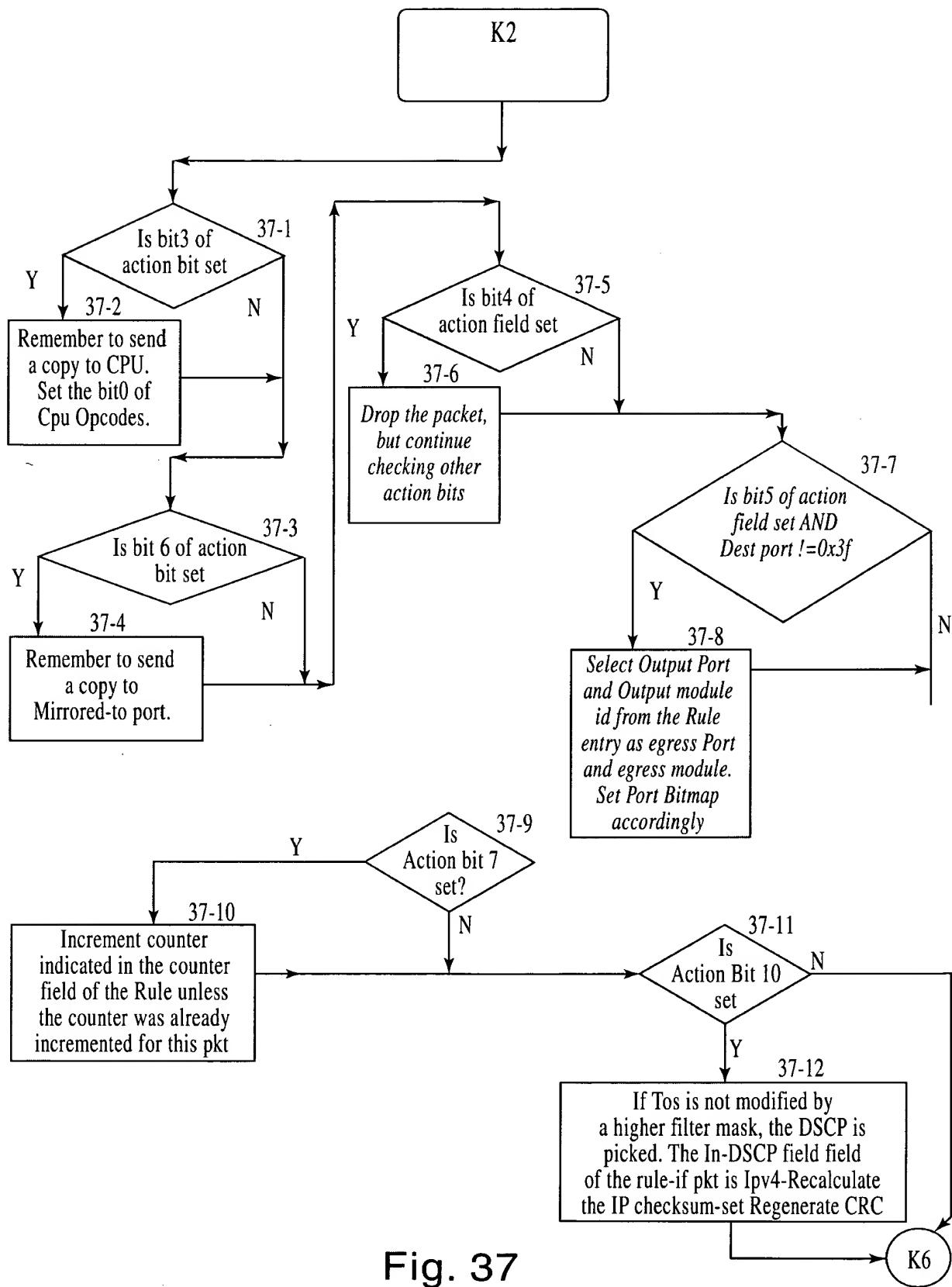


Fig. 37

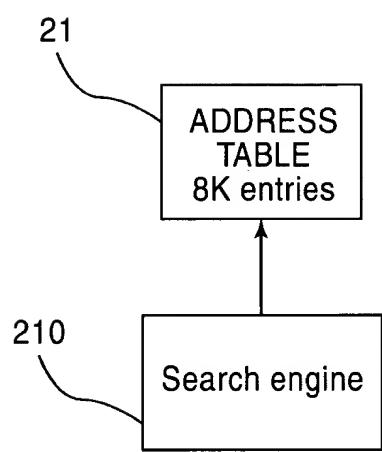


Fig.38

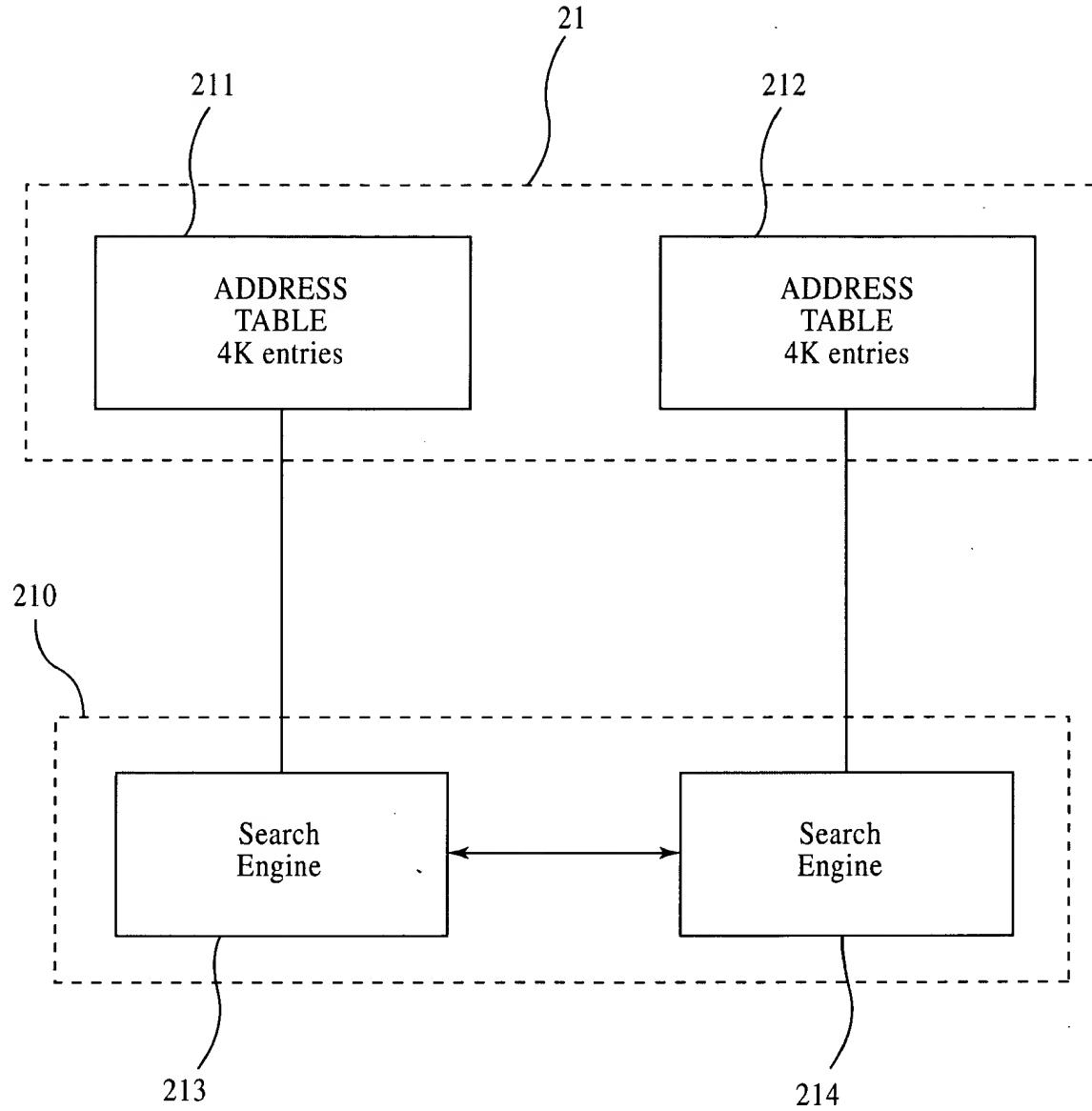


Fig.39



Fig.40a

address	entry
31	AF
30	AE
29	AD
28	AC
27	AB
26	AA
25	Z
24	Y
23	X
22	W
21	V
20	U
19	T
18	S
17	R
16	Q
15	P
14	O
13	N
12	M
11	L
10	K
9	J
8	I
7	H
6	G
5	F
4	E
3	D
2	C
1	B
0	A

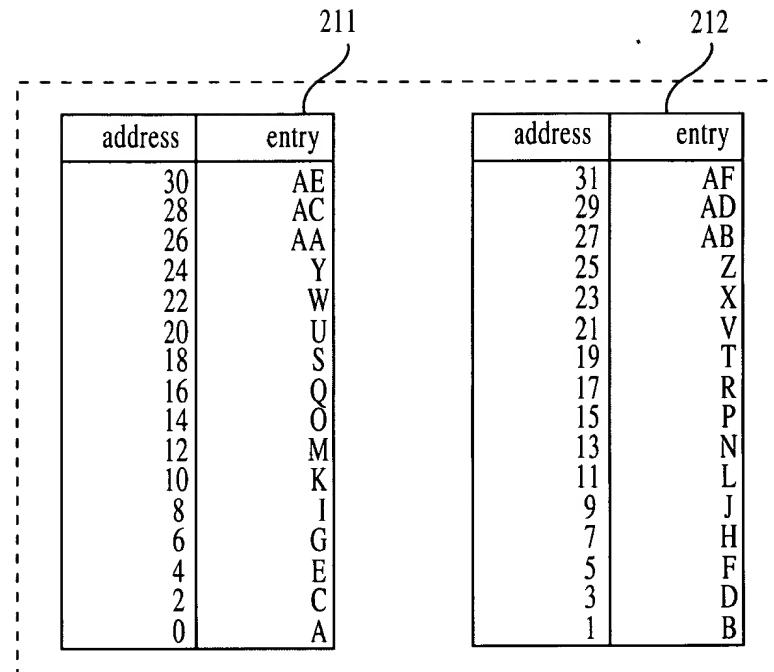


Fig.40b

21



Fig.41a

address	entry
31	NN
30	MM
29	LL
28	KK
27	JJ
26	GH
25	CF
24	CC
23	BE
22	BD
21	BC
20	BA
19	AC
18	AB
17	AA
16	Y
15	X
14	V
13	T
12	S
11	R
10	Q
9	N
8	M
7	L
6	K
5	J
4	G
3	E
2	D
1	C
0	B

211

address	entry
30	MM
28	KK
26	GH
24	CC
22	BD
20	BA
18	AB
16	Y
14	V
12	S
10	Q
8	M
6	K
4	G
2	D
0	B

212

address	entry
31	NN
29	LL
27	JJ
25	CF
23	BE
21	BC
19	AC
17	AA
15	X
13	T
11	R
9	N
7	L
5	J
3	E
1	C
0	B

Fig.41b

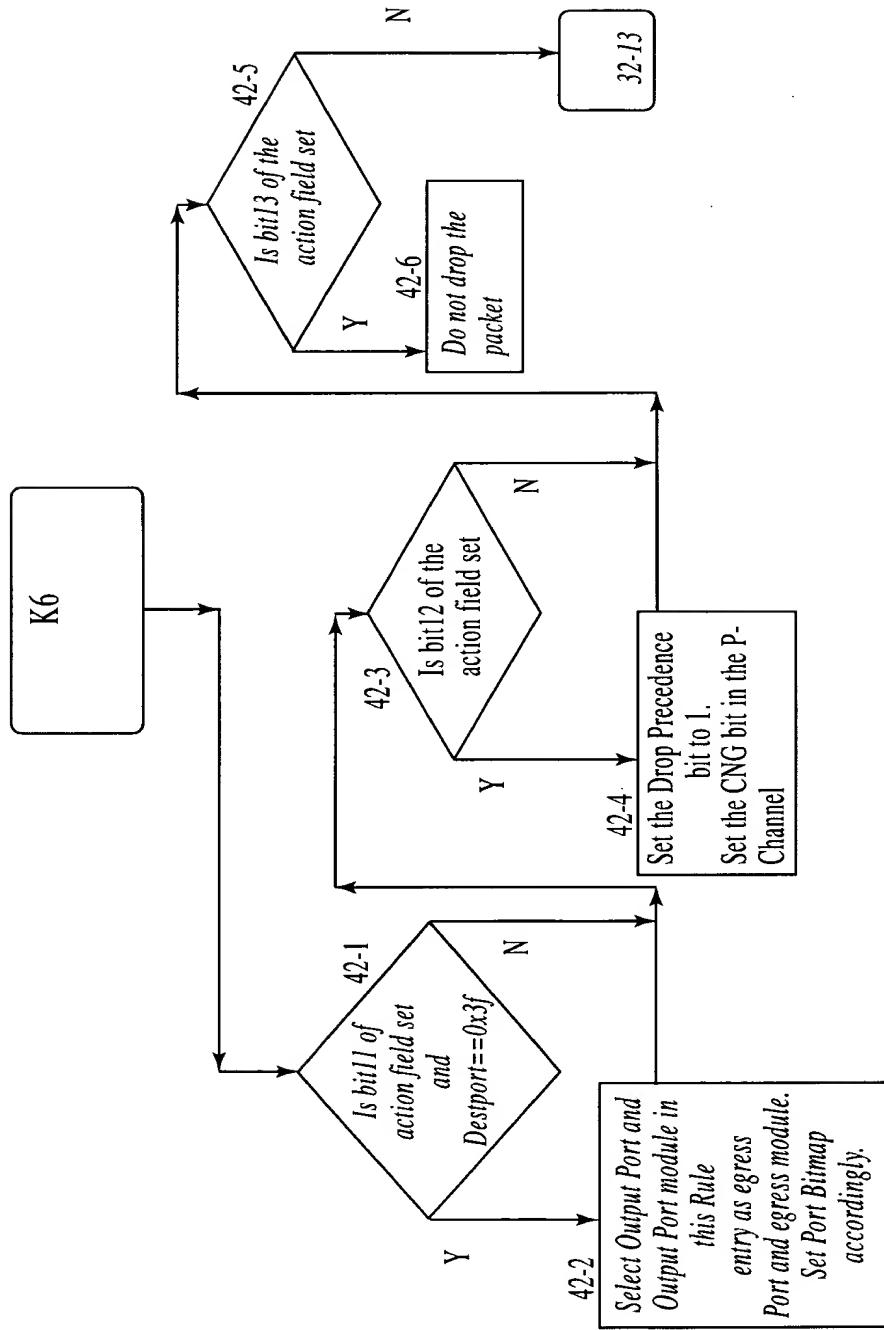


Fig.42

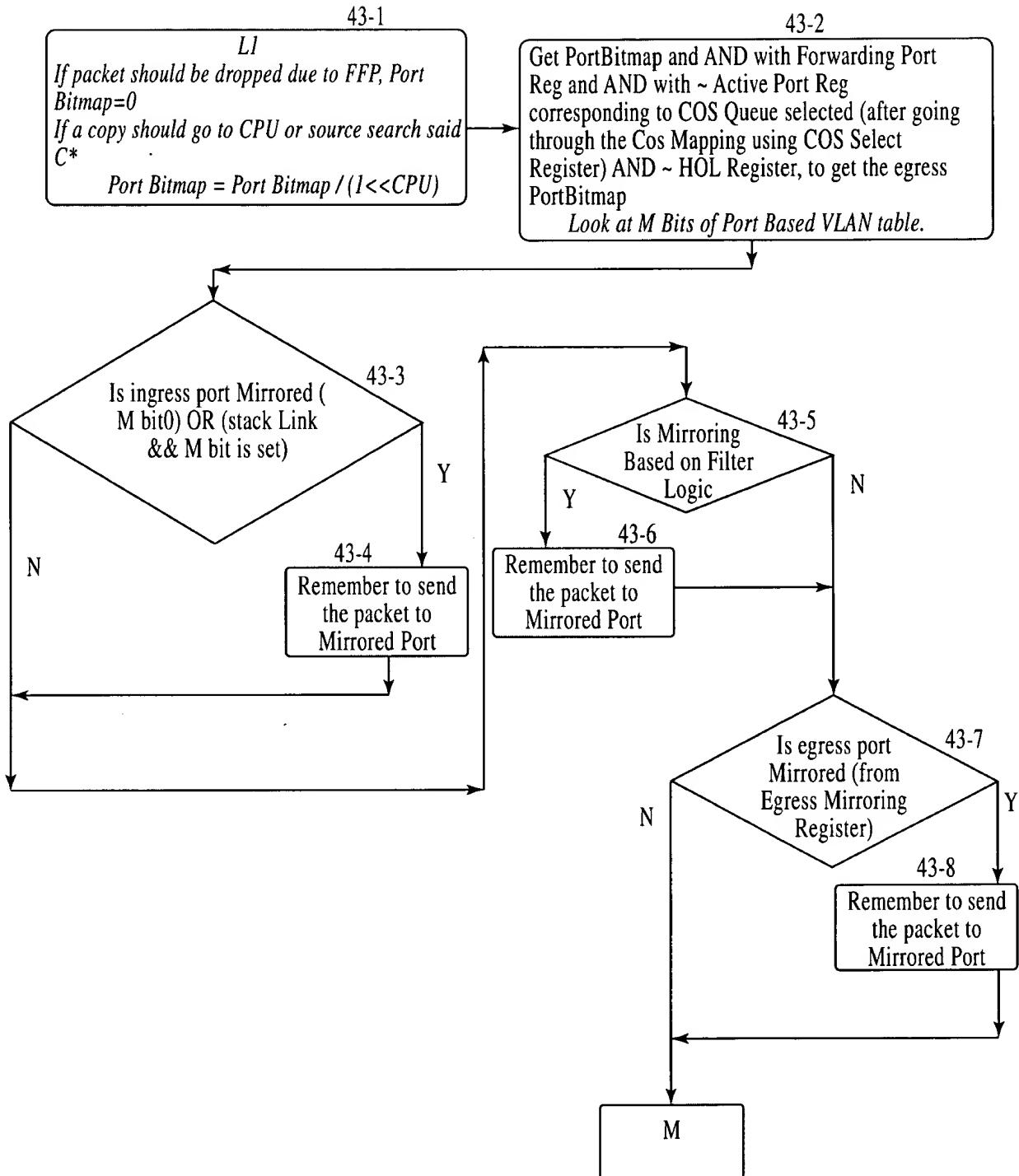
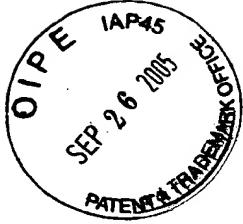


Fig.43

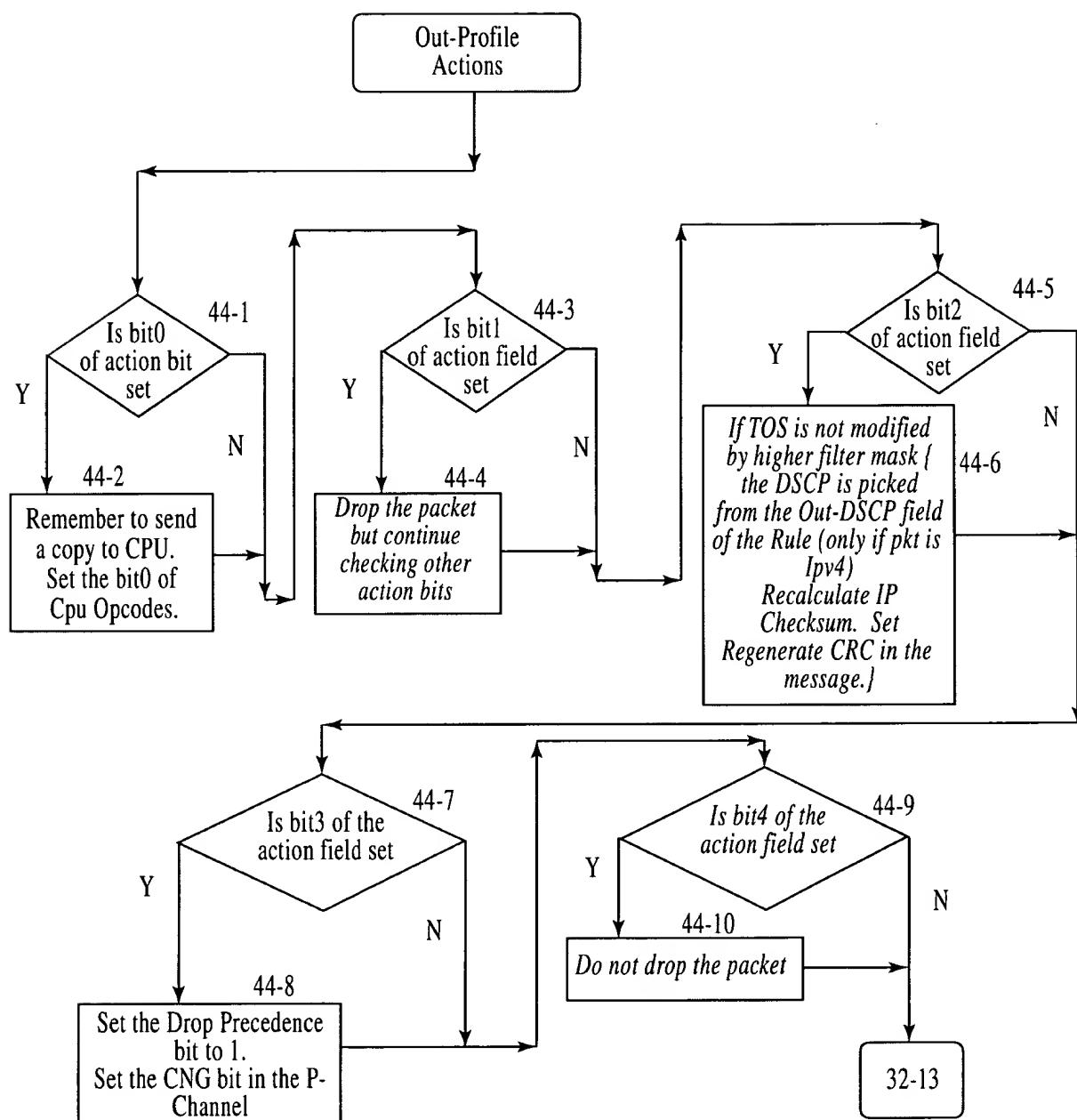


Fig.44

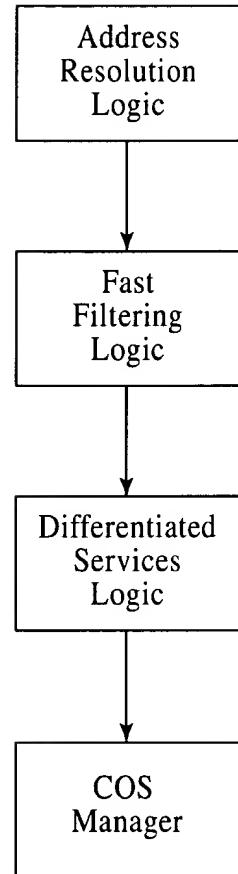


Fig.45

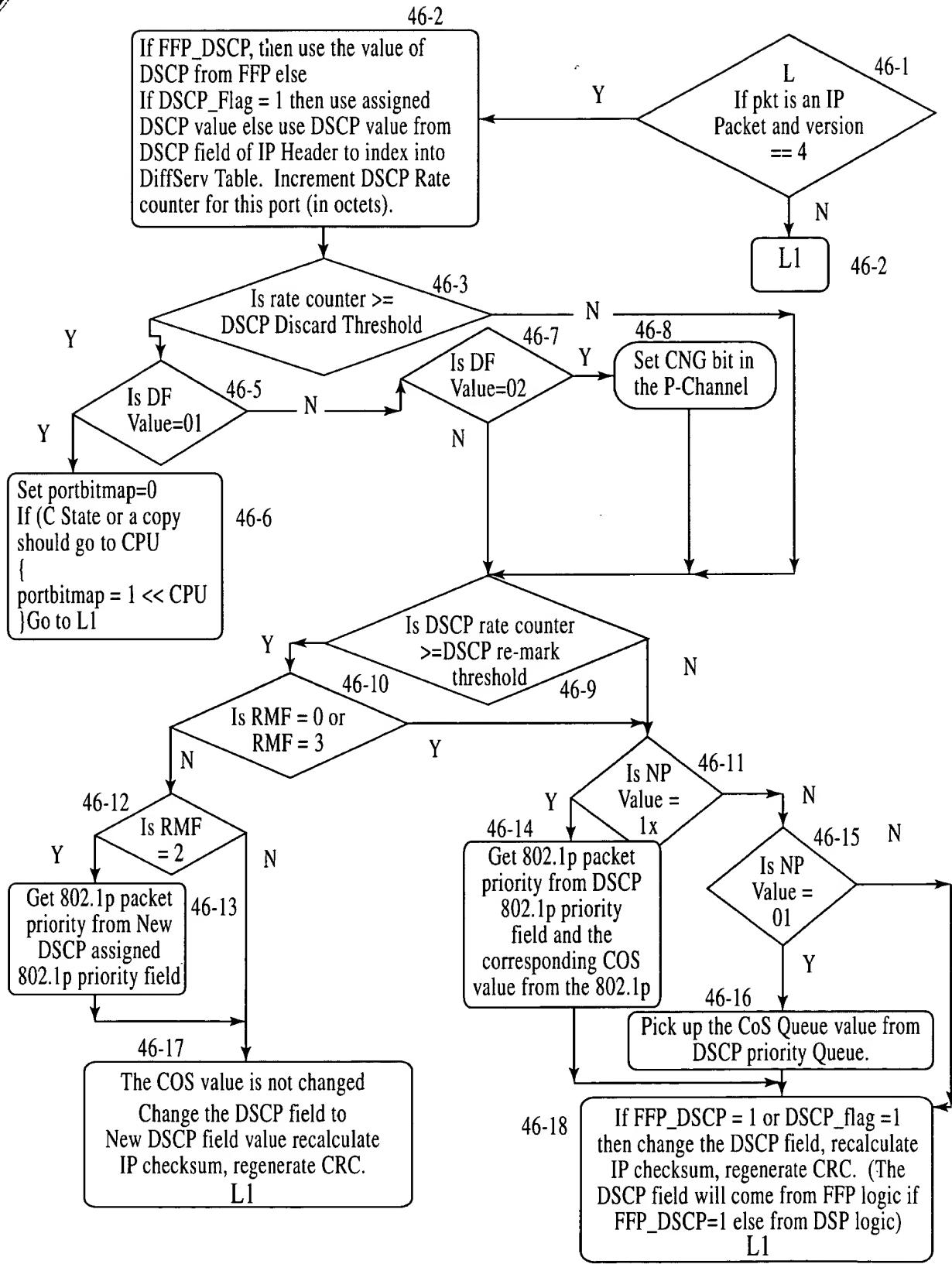


Fig.46



43-1

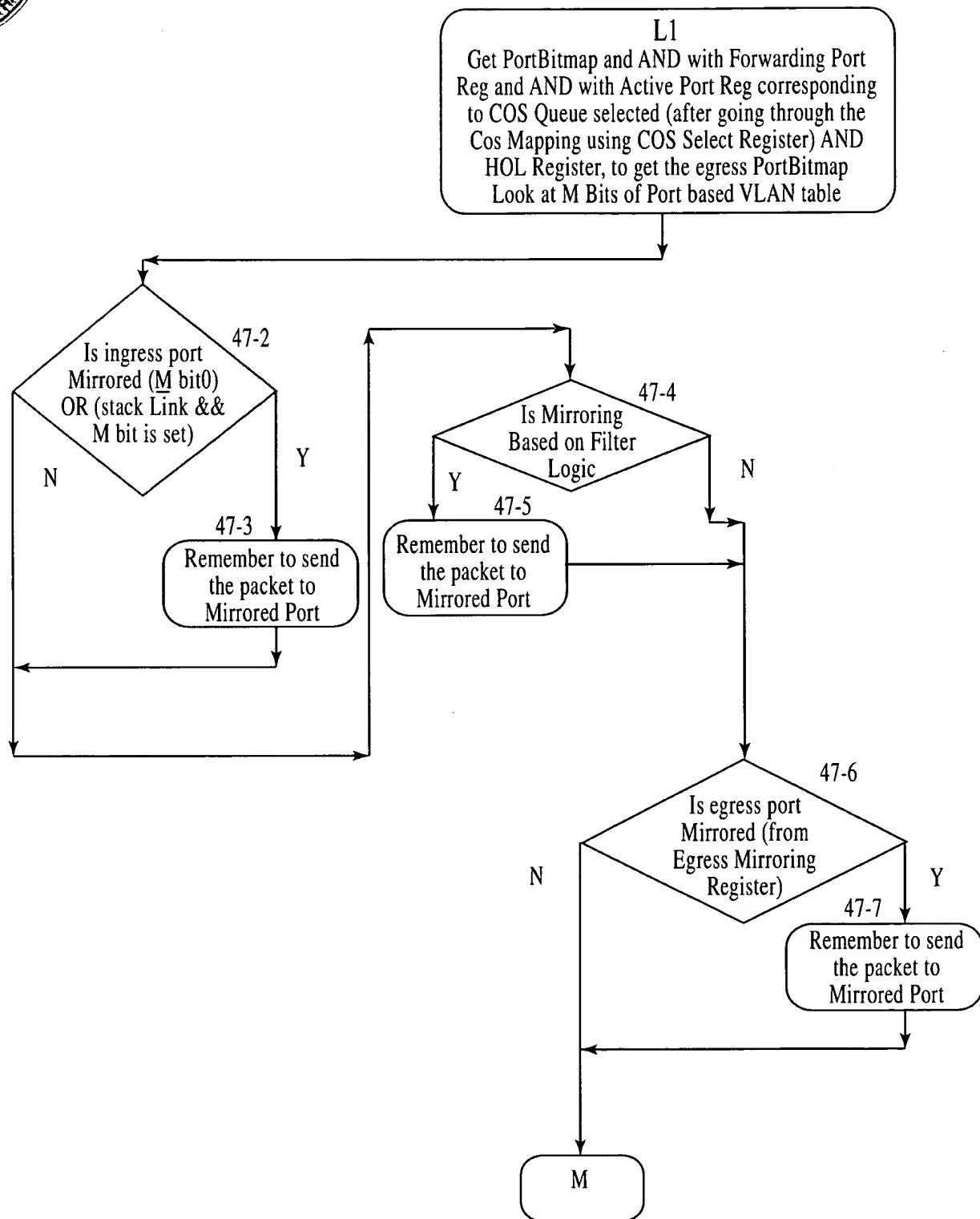


Fig.47